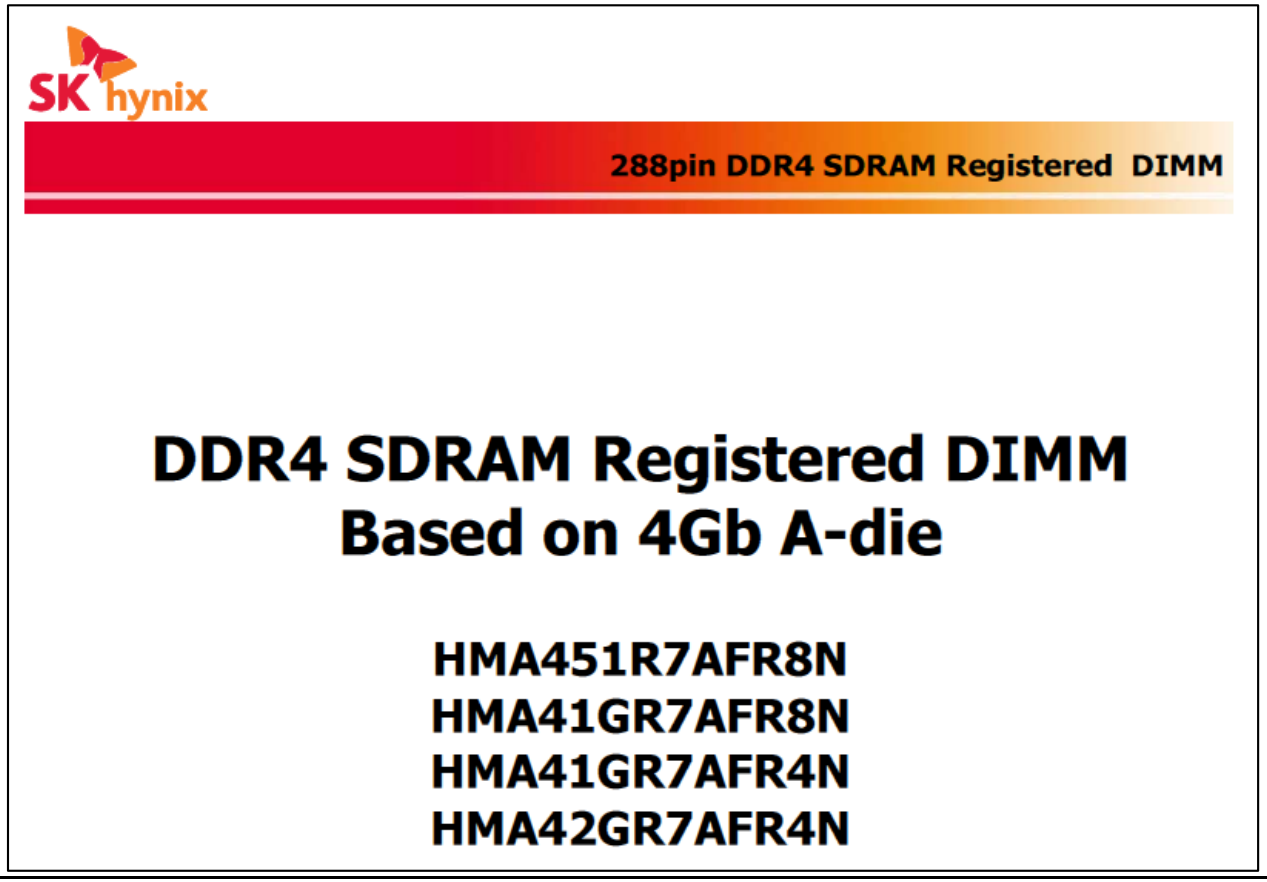
EXHIBIT 11

U.S. Patent No. 10,474,595
SK hynix HMA42GR7AFR4N-UHTD

U.S. Patent No. 10,474,595: Claim 1

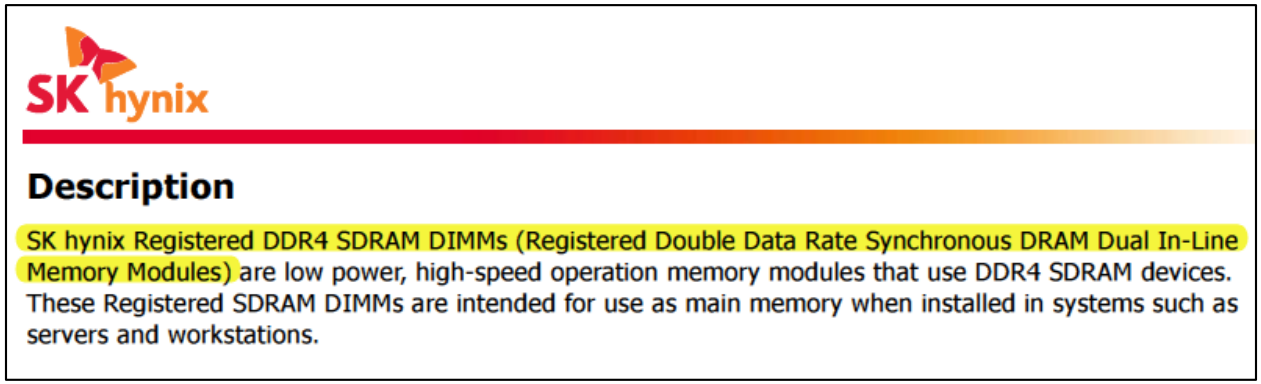
"1. A memory module operable with a memory controller of a host system, comprising:"

1. A memory module operable with a memory controller of a host system, comprising:	The SK hynix Products are memory modules operable with a memory controller of a host system. For example, the SK hynix Products are DDR4 registered dual in-line memory modules ("RDIMM"). (Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD). 

U.S. Patent No. 10,474,595: Claim 1

"1. A memory module operable with a memory controller of a host system, comprising:"

SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet, at 1.

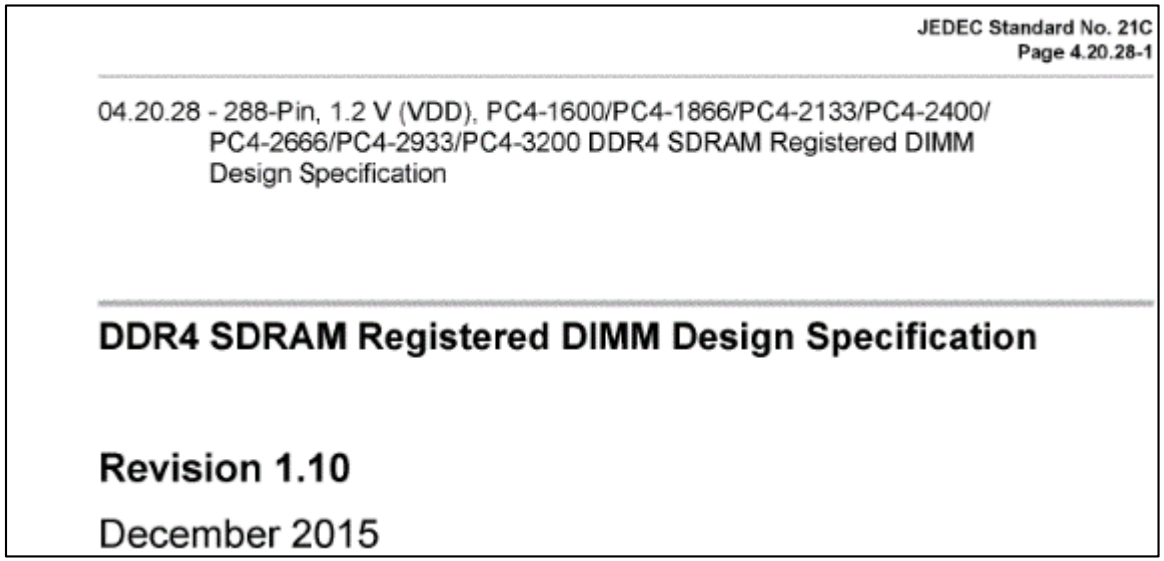


SK hynix

Description

SK hynix Registered DDR4 SDRAM DIMMs (Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Registered SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 3 (annotation added).



JEDEC Standard No. 21C
Page 4.20.28-1

04.20.28 - 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-2933/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification

DDR4 SDRAM Registered DIMM Design Specification

Revision 1.10

December 2015

JEDEC RDIMM Specification.

U.S. Patent No. 10,474,595: Claim 1

"1. A memory module operable with a memory controller of a host system, comprising:"

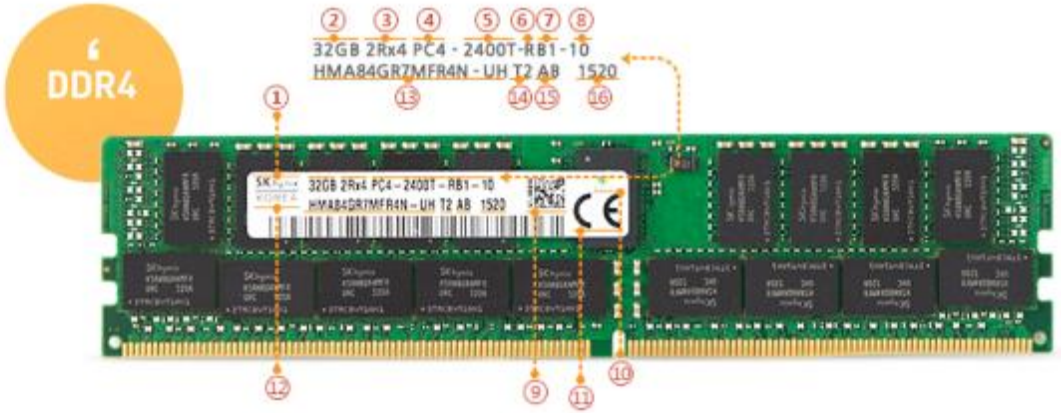
1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Registered, Double Data Rate, Synchronous SDRAM Dual In-Line Memory Modules (DDR4 SDRAM RDIMMs). These DDR4 Registered DIMMs (RDIMMs) are intended for use as main memory when installed in PCs.

JEDEC RDIMM Specification (annotation added).

The SK hynix HMA42GR7AFR4N-UHTD is manufactured according to JEDEC specifications:

Label Info. DDR4



See SKH DDR4 Module Label Info at 3.

(6)	Module Type	U : 288pin Unbuffered DIMM R : 288pin Registered DIMM S : 260 pin Unbuffered SO-DIMM L : 288pin LRDIMM N : 288pin NVDIMM
(7)	Gerber Revision	JEDEC Reference design file used for this design
(8)	SPD Revision	JEDEC SPD Revision Encoding and Additions level

See SKH DDR4 Module Label Info at 3.

U.S. Patent No. 10,474,595: Claim 1

"1. A memory module operable with a memory controller of a host system, comprising:"

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

The SK hynix Products are intended for use as main memory in systems such as servers and workstations.

JEDEC Standard No. 21C
Page 4.20.28-5

1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Registered, Double Data Rate, Synchronous SDRAM Dual In-Line Memory Modules (DDR4 SDRAM RDIMMs). These DDR4 Registered DIMMs (RDIMMs) are intended for use as main memory when installed in PCs.

JEDEC RDIMM Standard (annotation added).

SK hynix

Description

SK hynix Registered DDR4 SDRAM DIMMs (Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Registered SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 3 (annotations added).

The SK hynix Products are operable with a memory controller of a host system. For example, the SK hynix Products include a printed circuit board (PCB) for communicating signals between (e.g., to/from) the memory module and the memory controller of a host system.

U.S. Patent No. 10,474,595: Claim 1

"1. A memory module operable with a memory controller of a host system, comprising:"

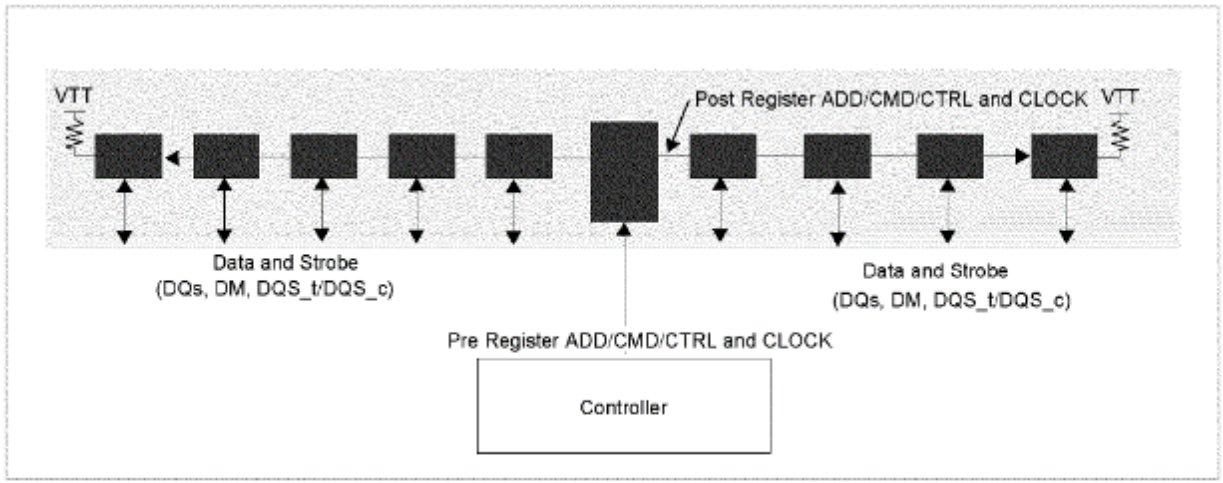


Figure 4 — Example RDIMM Topologies

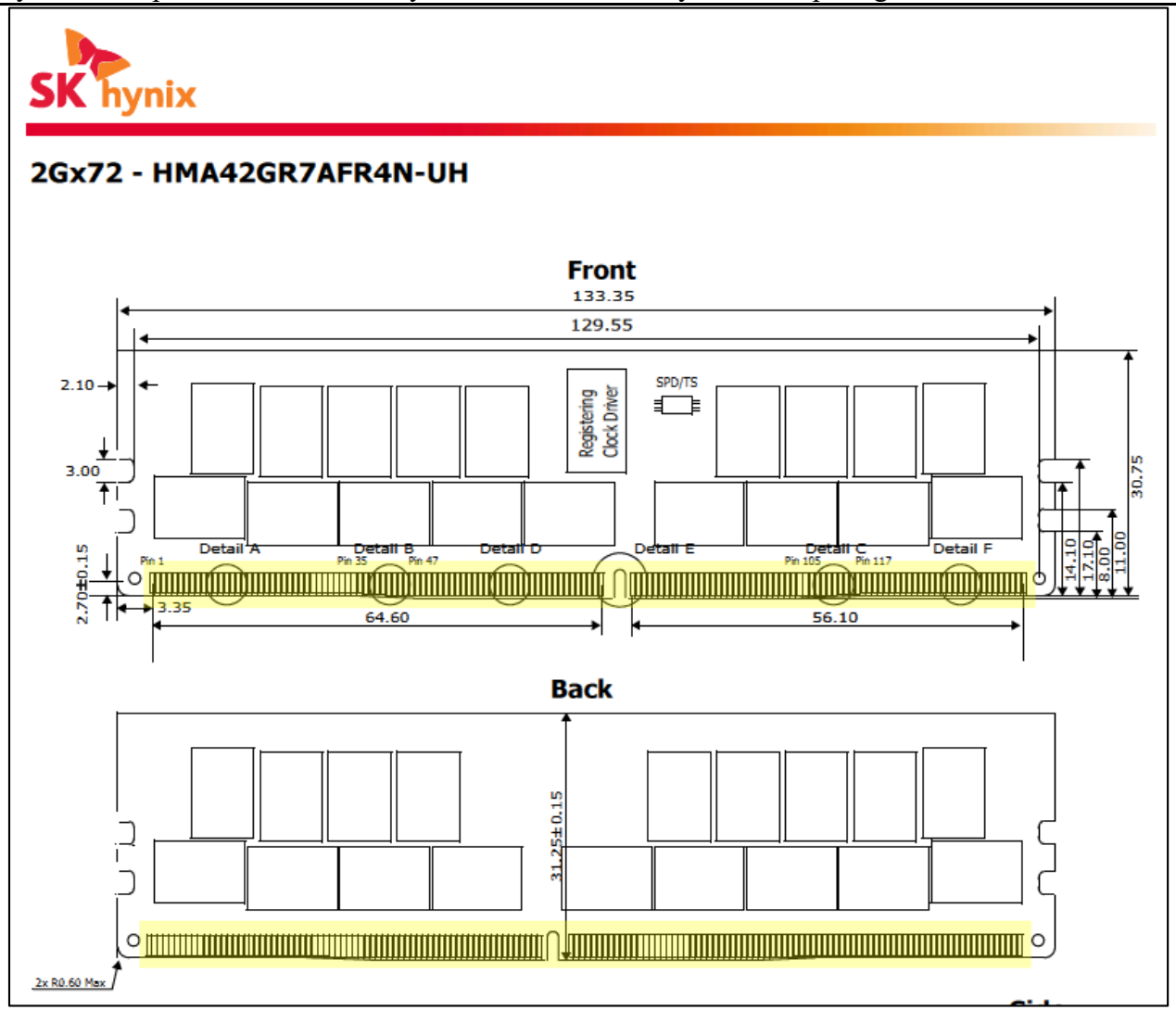
JEDEC RDIMM Specification.

For example, the SK hynix Products contain contacts for connecting to a memory controller of a computer system.

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

U.S. Patent No. 10,474,595: Claim 1

"1. A memory module operable with a memory controller of a host system, comprising:"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 81 (annotations added).

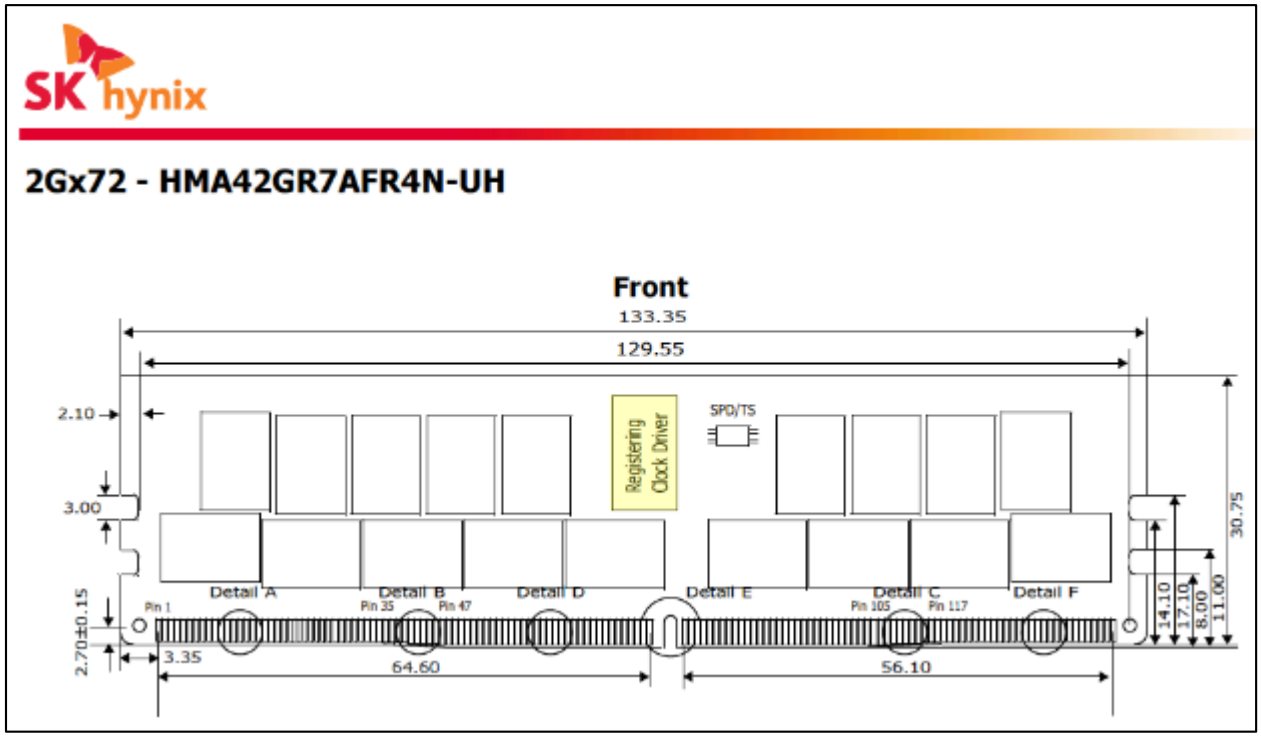
For example, the SK hynix include a JEDEC RCD01 compliant register clock driver ("RCD") that is operable with a memory controller of a host system.

> Some modules have lower current requirements. Any specific module must meet the SDRAM and DDR4RCD01 voltage requirements for its worst case supply currents.

U.S. Patent No. 10,474,595: Claim 1

"1. A memory module operable with a memory controller of a host system, comprising:"

See, e.g., JEDEC RDIMM Standard (annotation added).



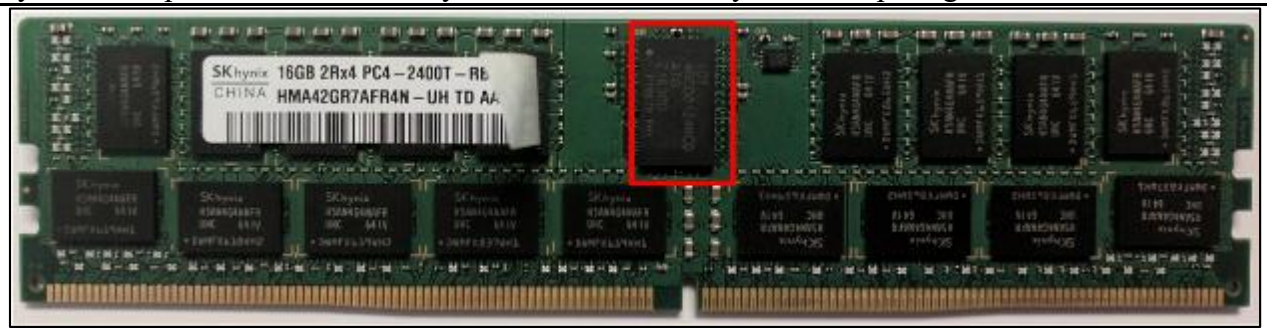
SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 81 (annotations added).

Specifically, the SK hynix Products contain an IDT 4RCD0124KC0 RCD.

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

U.S. Patent No. 10,474,595: Claim 1

"1. A memory module operable with a memory controller of a host system, comprising:"

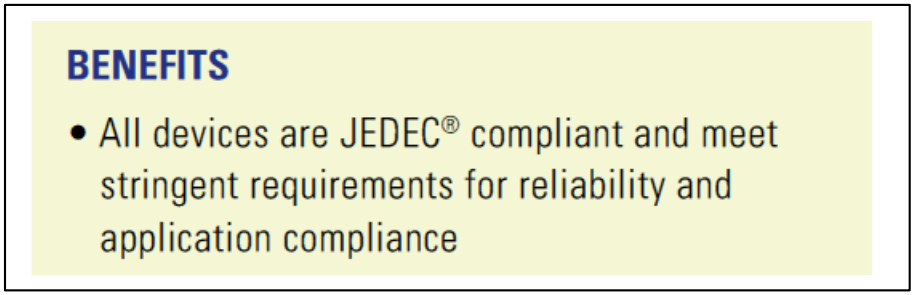


(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

The IDT 4RCD0124KC0 RCD is JEDEC Compliant.

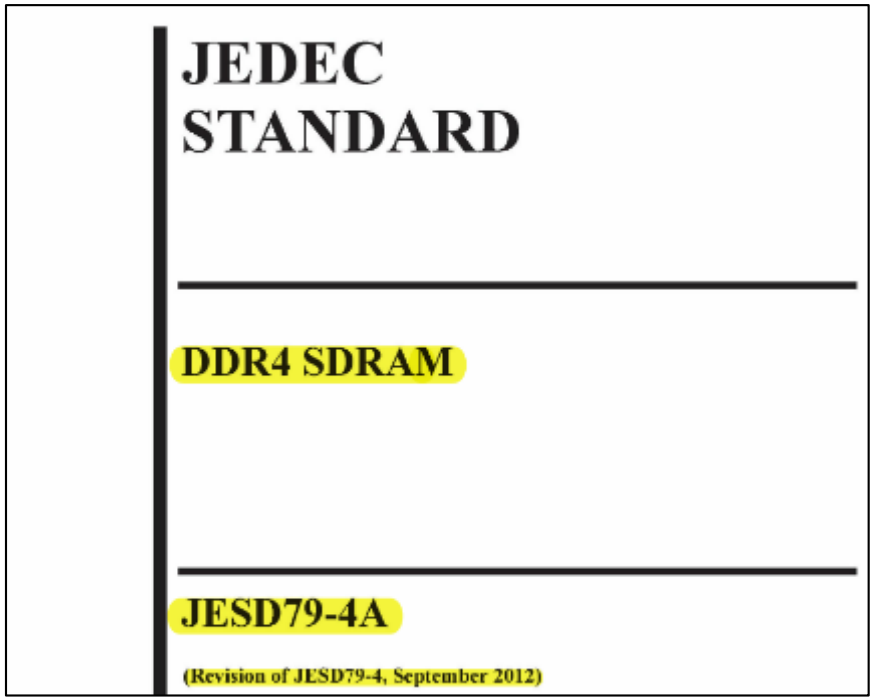
See 4RCD0124K DDR4 Register Clock Driver Webpage at 1.



IDT Leader in Server Memory Chipsets at 1.

U.S. Patent No. 10,474,595: Claim 1

"1. A memory module operable with a memory controller of a host system, comprising:"

	The SK hynix Products further comply with the JEDEC SDRAM Standard, JESD79-4.  JEDEC DDR4 SDRAM Specification (annotations added). *See also* SKH DDR4 Device Operation at 1. The RCD is operatively coupled to the memory controller of the host system.

U.S. Patent No. 10,474,595: Claim 1

"1. A memory module operable with a memory controller of a host system, comprising:"

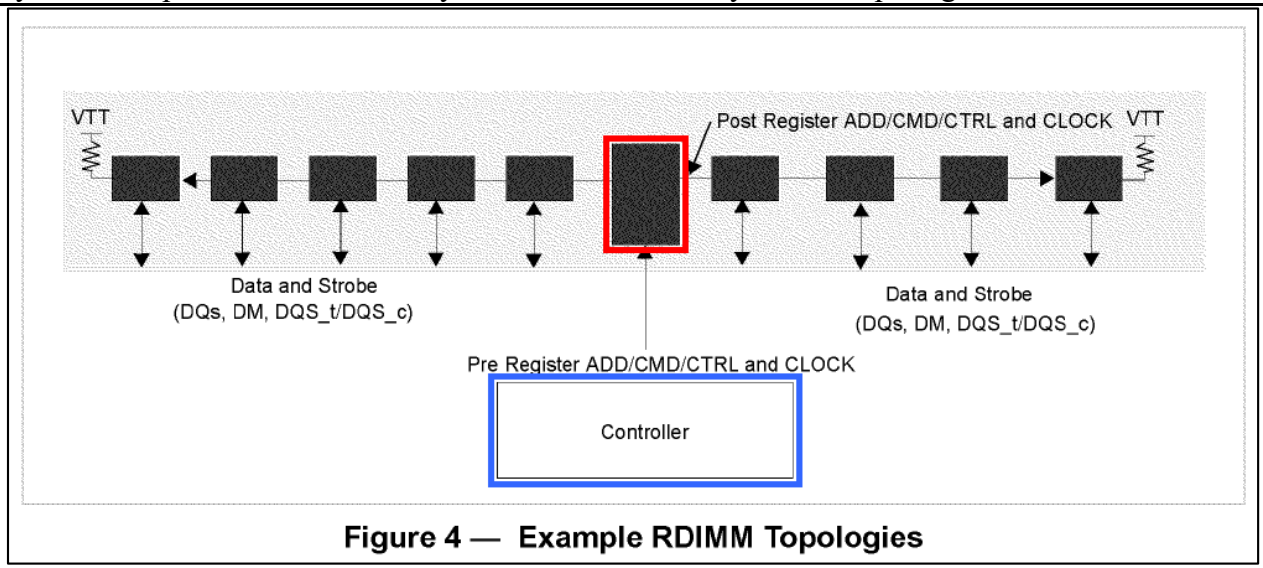


Figure 4 — Example RDIMM Topologies

JEDEC RDIMM Standard (annotation added).

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;	The SK hynix Products include a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections. The SK hynix Products include a printed circuit board (PCB) having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller. For example, the PCB of the SK hynix Products is configured to fit into a corresponding slot of the host system. SK hynix **Description** SK hynix Registered DDR4 SDRAM DIMMs (Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Registered SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations. SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 3 (annotation added). JEDEC Standard No. 21C Page 4.20.28-5 **1 Product Description** This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Registered, Double Data Rate, Synchronous SDRAM Dual In-Line Memory Modules (DDR4 SDRAM RDIMMs). These DDR4 Registered DIMMs (RDIMMs) are intended for use as main memory when installed in PCs. JEDEC RDIMM Standard (annotation added).

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

For example, as illustrated in the figures below, the SK hynix Products include a printed circuit board (PCB) having edge connections for communicating signals between (e.g., to/from) the memory module and the memory controller of the host system, e.g., electrical communication between the memory module and the memory controller.

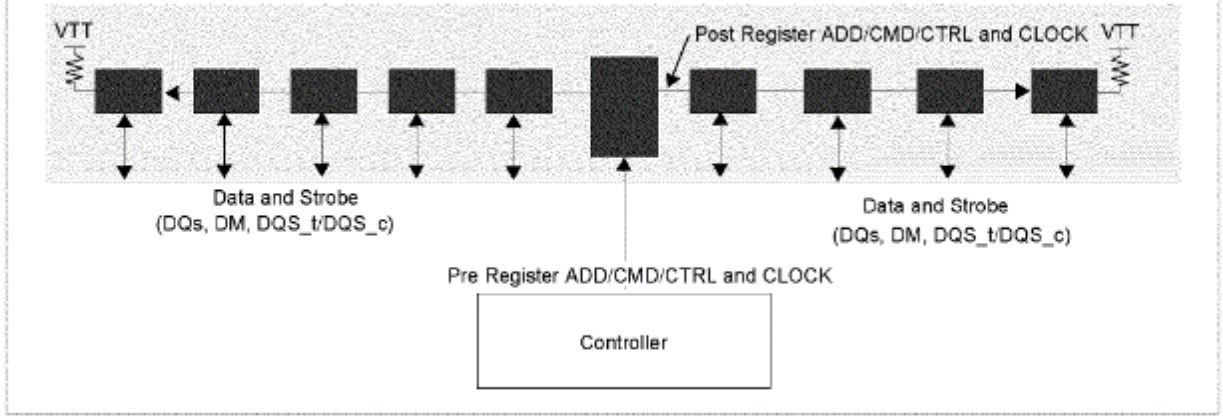


Figure 4 — Example RDIMM Topologies

JEDEC RDIMM Standard.

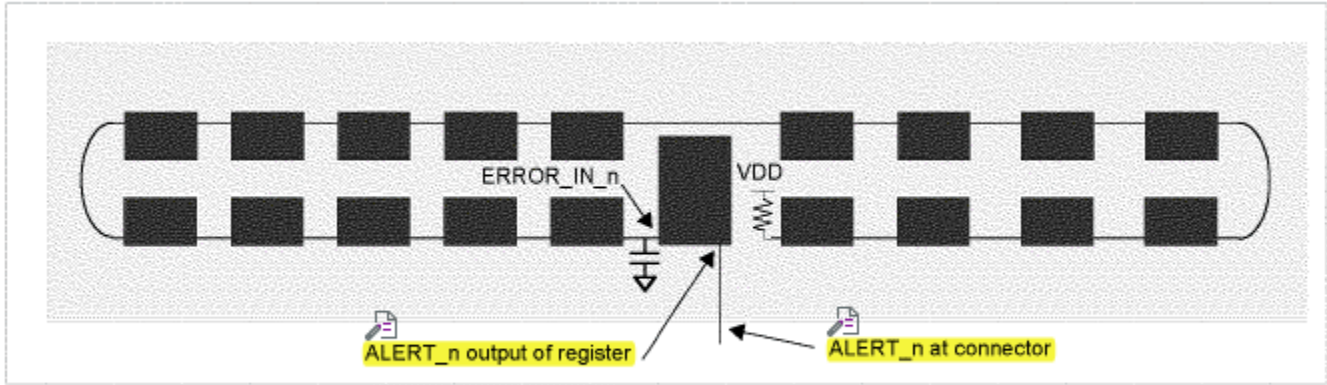


Figure 16 — Example Wiring of the ALERT_n Function

JEDEC RDIMM Standard (annotations added).

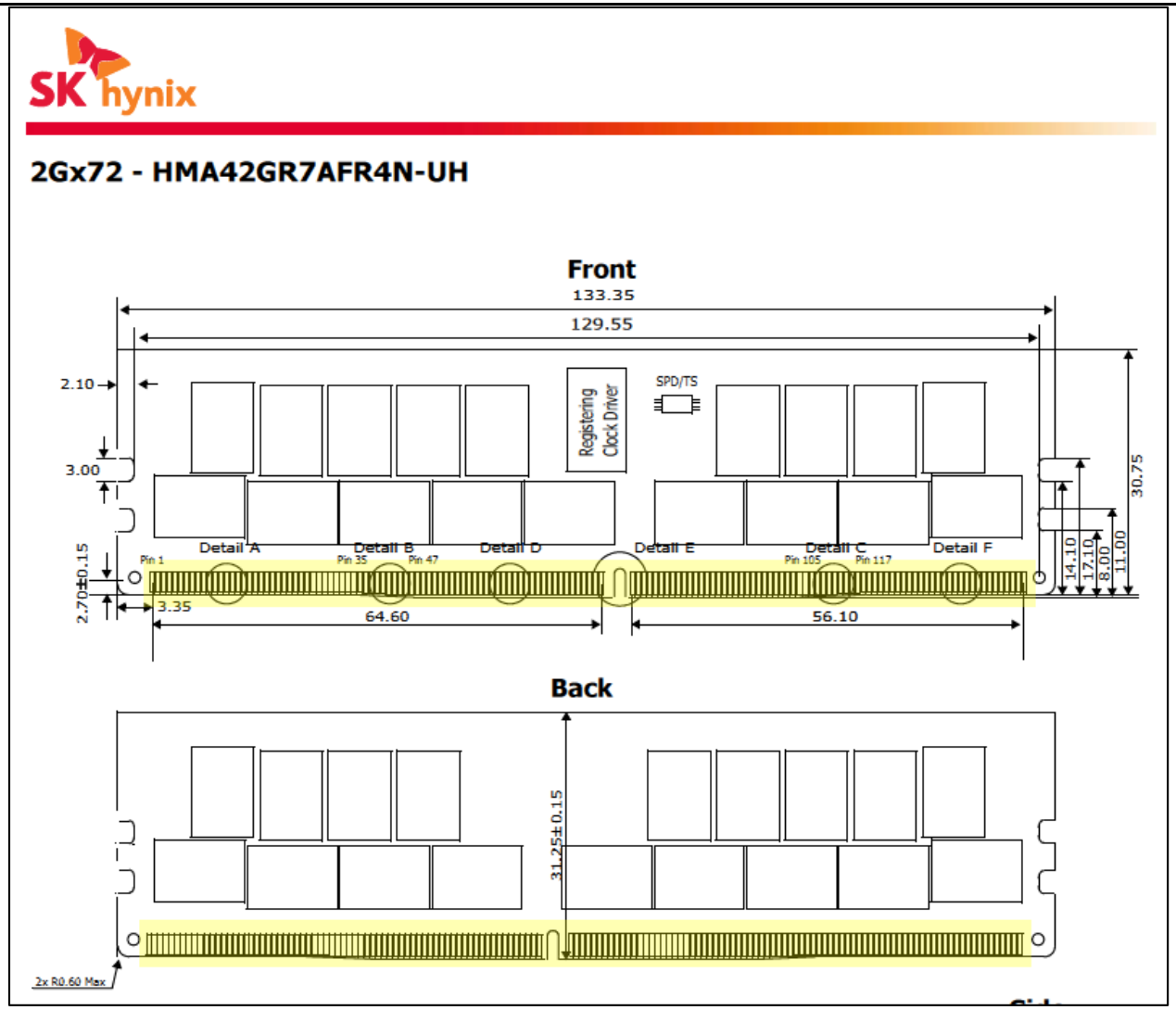
U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

	For example, the SK hynix Products contain contacts (e.g., edge connections) for connecting to a memory controller of a computer system. (Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 81 (annotations added).

The edge connections of the SK hynix Products include a first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections.

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

JEDEC Standard No. 21C
Page 4.20.28-10

Table 5 — DDR4 288 Pin RDIMM Pin Wiring Assignments

Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
12 V, NC	1	145	12 V, NC	CK0_t	74	218	CK1_t
VSS	2	146	VREFCA	CK0_c	75	219	CK1_c
DQ4	3	147	VSS	VDD	76	220	VDD
VSS	4	148	DQ5	VTT	77	221	VTT
DQ0	5	149	VSS	KEY			
VSS	6	150	DQ1				
TDQS9_t, DQS9_t, DM0_n, DBI0_n, NC	7	151	VSS	EVENT_n	78	222	PARITY
TDQS9_c, DQS9_c, NC	8	152	DQS0_c	A0	79	223	VDD
VSS	9	153	DQS0_t	VDD	80	224	BA1
DQ6	10	154	VSS	BA0	81	225	A10/AP
VSS	11	155	DQ7	RAS_n/A16	82	226	VDD
DQ2	12	156	VSS	VDD	83	227	RFU
VSS	13	157	DQ3	CS0_n	84	228	WE_n/A14
DQ12	14	158	VSS	VDD	85	229	VDD

JEDEC RDIMM Standard (showing, for example, WE_n, A0, DQ4).

ACT_n	62	206	VDD	TDQS16_c, DQS16_c, NC	133	277	DQS7_c
BG0	63	207	BG1	VSS	134	278	DQS7_t
VDD	64	208	ALERT_n	DQ62	135	279	VSS
A12/BC_n	65	209	VDD	VSS	136	280	DQ63
A9	66	210	A11	DQ58	137	281	VSS
VDD	67	211	A7	VSS	138	282	DQ59
A8	68	212	VDD	SA0	139	283	VSS
A6	69	213	A5	SA1	140	284	VDDSPD
VDD	70	214	A4	SCL	141	285	SDA
A3	71	215	VDD	VPP	142	286	VPP
A1	72	216	A2	VPP	143	287	VPP
VDD	73	217	VDD	RFU	144	288	VPP

JEDEC RDIMM Standard (showing, for example, ALERT_n).

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

SK hynix

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
37	VSS	181	DQ29	108	DQ40	252	VSS
38	DQ24	182	VSS	109	VSS	253	DQ41
39	VSS	183	DQ25	110	TDQS14_t, DQS14_t, DM5_n, DBI5_n	254	VSS
40	TDQS12_t, DQS12_t, DM3_n, DBI3_n	184	VSS	111	TDQS14_c, DQS14_c	255	DQS5_c
41	TDQS12_c, DQS12_c	185	DQS3_c	112	VSS	256	DQS5_t
42	VSS	186	DQS3_t	113	DQ46	257	VSS
43	DQ30	187	VSS	114	VSS	258	DQ47
44	VSS	188	DQ31	115	DQ42	259	VSS
45	DQ26	189	VSS	116	VSS	260	DQ43
46	VSS	190	DQ27	117	DQ52	261	VSS
47	CB4	191	VSS	118	VSS	262	DQ53
48	VSS	192	CB5	119	DQ48	263	VSS
49	CB0	193	VSS	120	VSS	264	DQ49
50	VSS	194	CB1	121	TDQS15_t, DQS15_t, DM6_n, DBI6_n	265	VSS
51	TDQS17_t, DQS17_t, DM8_n, DBI8_n	195	VSS	122	TDQS15_c, DQS15_c	266	DQS6_c
52	TDQS17_c, DQS17_c	196	DQS8_c	123	VSS	267	DQS6_t
53	VSS	197	DQS8_t	124	DQ54	268	VSS
54	CB6	198	VSS	125	VSS	269	DQ55
55	VSS	199	CB7	126	DQ50	270	VSS
56	CB2	200	VSS	127	VSS	271	DQ51
57	VSS	201	CB3	128	DQ60	272	VSS
58	RESET_n	202	VSS	129	VSS	273	DQ61
59	VDD	203	CKE1, NC	130	DQ56	274	VSS
60	CKE0	204	VDD	131	VSS	275	DQ57
61	VDD	205	RFU	132	TDQS16_t, DQS16_t, DM7_n, DBI7_n	276	VSS
62	ACT_n	206	VDD	133	TDQS16_t, DQS16_c	277	DQS7_c
63	BG0	207	BG1	134	VSS	278	DQS7_t
64	VDD	208	ALERT_n	135	DQ62	279	VSS
65	A12/BC_n	209	VDD	136	VSS	280	DQ63
66	A9	210	A11	137	DQ58	281	VSS
67	VDD	211	A7	138	VSS	282	DQ59
68	A8	212	VDD	139	SA0	283	VSS
69	A6	213	A5	140	SA1	284	VDDSPD
70	VDD	214	A4	141	SCL	285	SDA
71	A3	215	VDD	142	VPP	286	VPP
72	A1	216	A2	143	VPP	287	VPP
73	VDD	217	VDD	144	RFU	288	VPP

SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 10 (showing separate pin connections for data, address, control, and ALERT_n).

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

For example, the SK hynix Products include first edge connections for communicating data signals between the memory module and the memory controller of the host system. For example, the SK hynix Products include the following input/output pins:

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I^2C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I^2C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I^2C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS9_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	DM0_n-DM8_n	Data Mask
DQS0_c–DQS17_c	Data Buffer data strobes	RESET_n	Set Register and SDRAMs to a Known State

DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

DQS0_t-DQS17_t, DQS0_c-DQS17_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

JEDEC RDIMM Standard.
See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 5, 7.

The DQ and DQS signals are used to communicate data signals between the memory module and the memory controller of the host system.

JEDEC Standard No. 21C
Page 4.20.28-19

6 DIMM Design Details

6.1 Signal Groups

This specification categorizes DDR4 SDRAM signals into six groups. Figure 4 illustrates the DIMM wiring. All signal groups, except DQ, implement a fly-by topology.

The signal groups are:

1. DQ and DQS signals connector to SDRAM

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

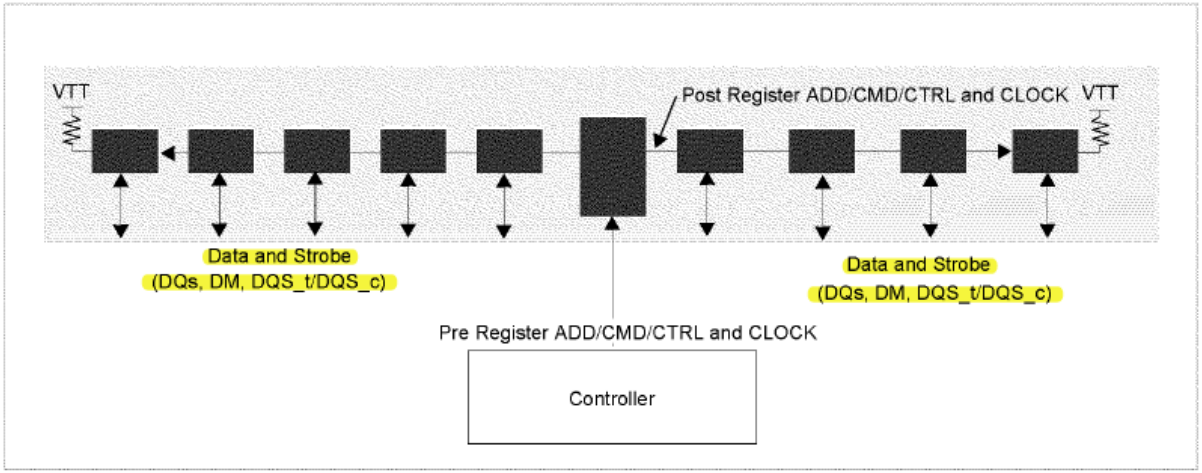


Figure 4 — Example RDIMM Topologies

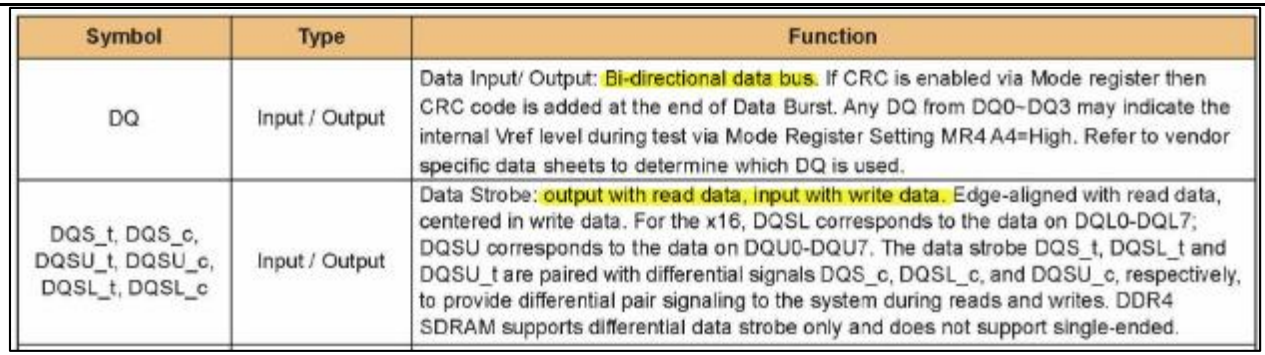
JEDEC RDIMM Standard (annotations added).

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

JEDEC DDR4 SDRAM Specification (annotations added).
See also SKH DDR4 Device Operation at 7.

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

	 JEDEC DDR4 SDRAM Specification (annotations added). *See also* SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 7.

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

JEDEC Standard No. 79-4A
Page 86

4.24.1.2 READ Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 67 and is applied when the DLL is enabled and locked.

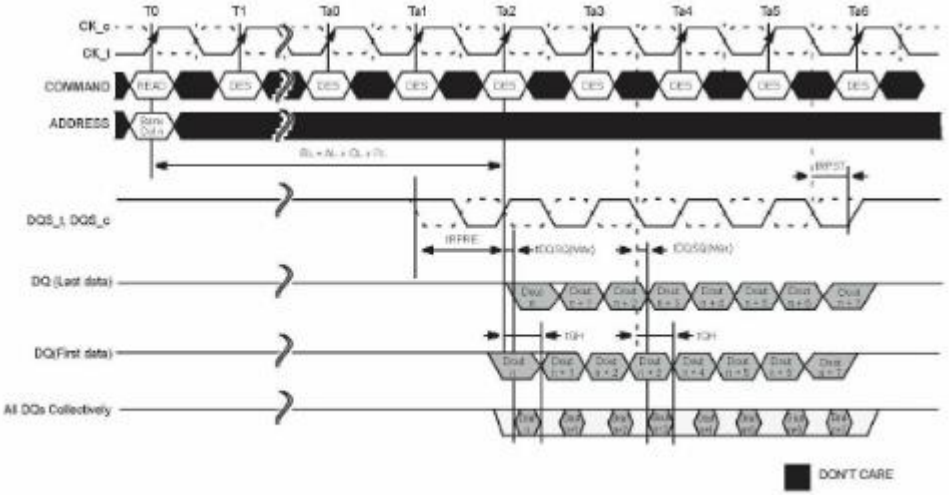
Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

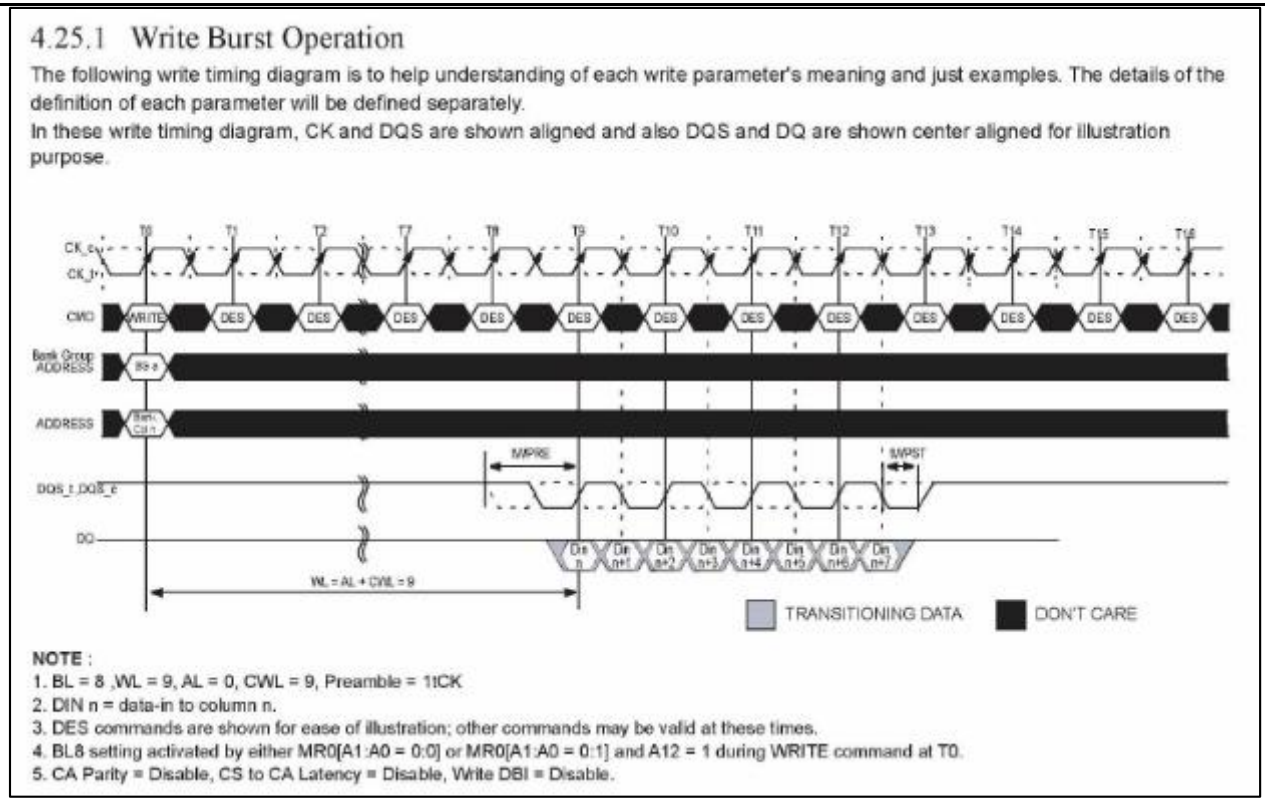
tDQSQ: both rising/falling edges of DQS, no tAC defined.



See, e.g., JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 97.

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"



4.25.1 Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.

In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.

NOTE :
1. BL = 8 ,WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

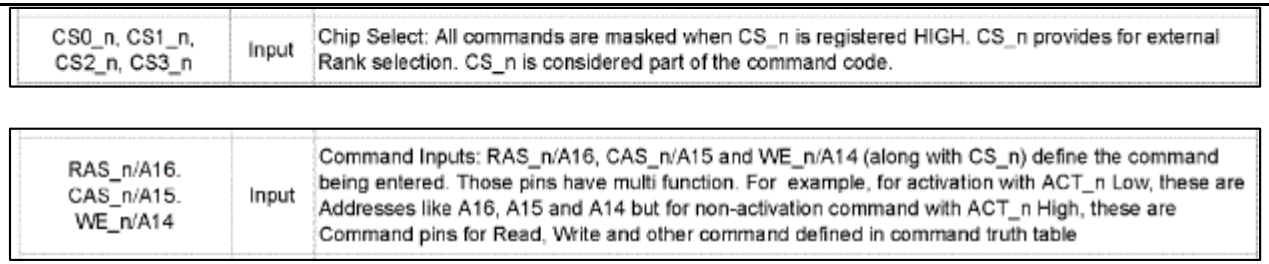
See, e.g., JEDEC DDR4 SDRAM Specification.
See also JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 126, 94-144.

The SK hynix Products also include second edge connections for communicating address and control signals from the memory controller of the host system. For example, the SK hynix Products include the following input pins:

A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.

U.S. Patent No. 10,474,595: Claim 1

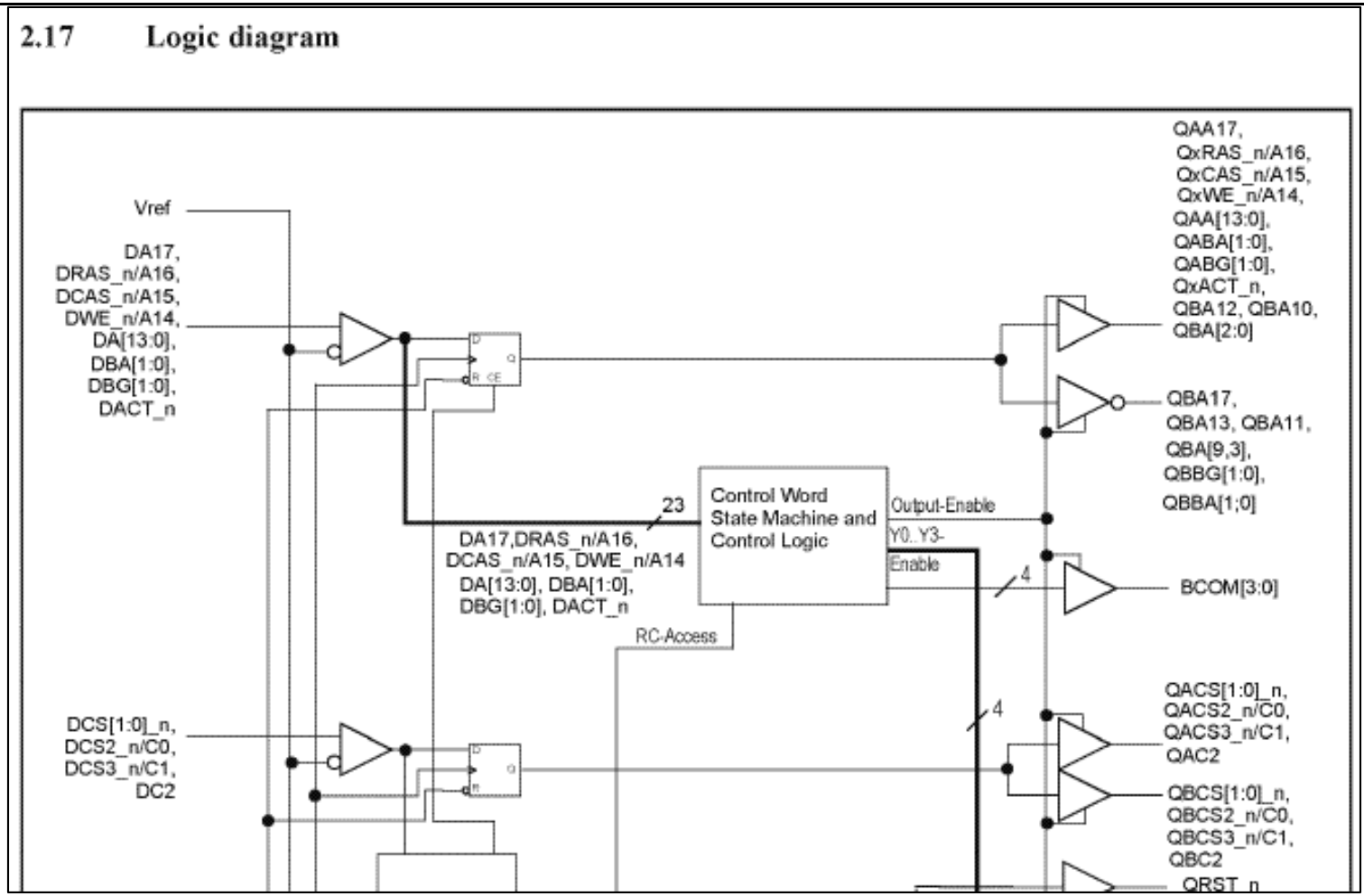
"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

	 JEDEC RDIMM Standard. *See also* SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 6.

CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"



See JEDEC RCD01 Specification.

The PCB further includes an error edge connection in addition to the first set of edge connections and the second set of edge connections. For example, the SK hynix Products include the ALERT_n pin.

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

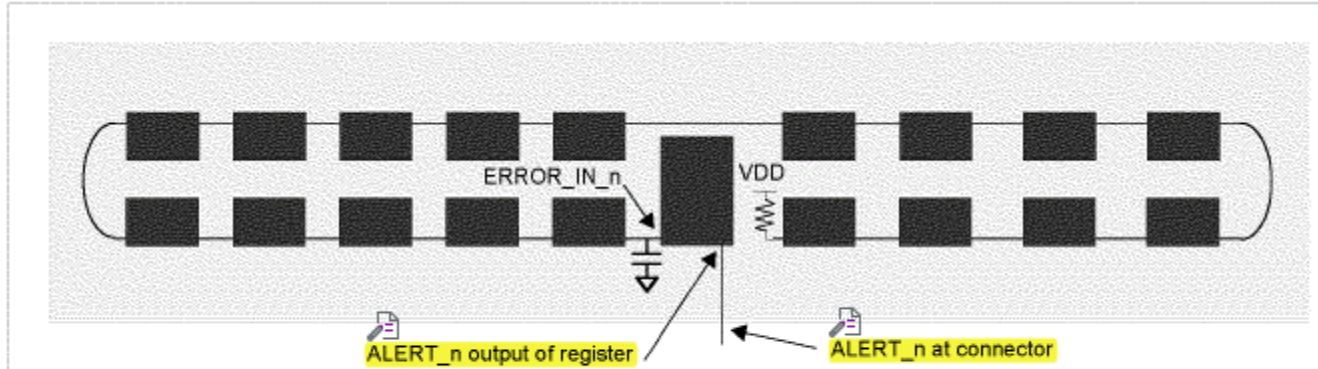


Figure 16 — Example Wiring of the ALERT_n Function

JEDEC RDIMM Standard (annotations added).

U.S. Patent No. 10,474,595: Claim 1

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I²C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I²C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I²C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS9_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	DM0_n-DM8_n	Data Mask
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred.
CK0_t, CK1_t	Register clock input (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clocks input (negative line of differential pair)	RFU	Reserved for future use

JEDEC RDIMM Standard (annotations added).

ALERT_n	Output (Input)	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system.

JEDEC RDIMM Standard.

U.S. Patent No. 10,474,595: Claim 1

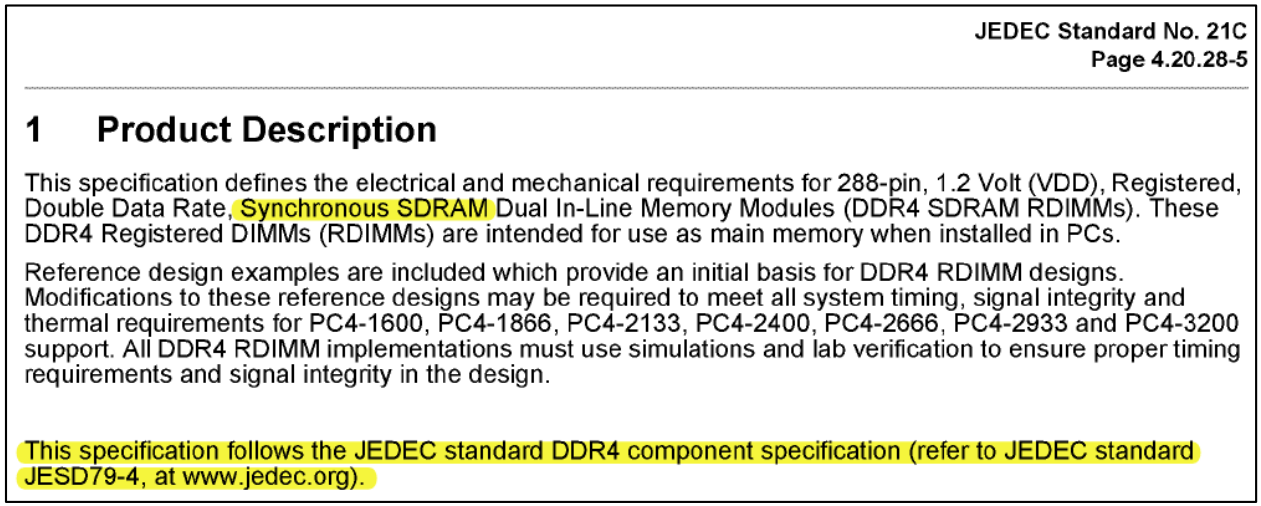
"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
TDQS12_t, DQS12_t, DM3_n, DBI3_n, NC	40	184	VSS	TDQS14_c, DQS14_c, NC	111	255	DQS5_c
TDQS12_c, DQS12_c, NC	41	185	DQS3_c	VSS	112	256	DQS5_t
VSS	42	186	DQS3_t	DQ46	113	257	VSS
DQ30	43	187	VSS	VSS	114	258	DQ47
VSS	44	188	DQ31	DQ42	115	259	VSS
DQ26	45	189	VSS	VSS	116	260	DQ43
VSS	46	190	DQ27	DQ52	117	261	VSS
CB4, NC	47	191	VSS	VSS	118	262	DQ53
VSS	48	192	CB5, NC	DQ48	119	263	VSS
CB0, NC	49	193	VSS	VSS	120	264	DQ49
VSS	50	194	CB1, NC	TDQS15_t, DQS15_t, DM6_n, DBI6_n, NC	121	265	VSS
TDQS17_t, DQS17_t, DM8_n, DBI8_n, NC	51	195	VSS	TDQS15_c, DQS15_c, NC	122	266	DQS6_c
TDQS17_c, DQS17_c, NC	52	196	DQS8_c	VSS	123	267	DQS6_t
VSS	53	197	DQS8_t	DQ54	124	268	VSS
CB6, NC	54	198	VSS	VSS	125	269	DQ55
VSS	55	199	CB7, NC	DQ50	126	270	VSS
CB2, NC	56	200	VSS	VSS	127	271	DQ51
VSS	57	201	CB3, NC	DQ60	128	272	VSS
RESET_n	58	202	VSS	VSS	129	273	DQ61
VDD	59	203	CKE1, NC	DQ56	130	274	VSS
CKE0	60	204	VDD	VSS	131	275	DQ57
VDD	61	205	RFU	TDQS16_t, DQS16_t, DM7_n, DBI7_n, NC	132	276	VSS
ACT_n	62	206	VDD	TDQS16_c, DQS16_c, NC	133	277	DQS7_c
BG0	63	207	BG1	VSS	134	278	DQS7_t
VDD	64	208	ALERT_n	DQ62	135	279	VSS
A12/BC_n	65	209	VDD	VSS	136	280	DQ63
A9	66	210	A11	DQ58	137	281	VSS
VDD	67	211	A7	VSS	138	282	DQ59
A8	68	212	VDD	SA0	139	283	VSS
A6	69	213	A5	SA1	140	284	VDDSPD
VDD	70	214	A4	SCL	141	285	SDA
A3	71	215	VDD	VPP	142	286	VPP
A1	72	216	A2	VPP	143	287	VPP
VDD	73	217	VDD	RFU	144	288	VPP

JEDEC RDIMM Standard (annotations added) (showing Alert_n at pin 208, separate and distinct from control, address, and data pins / edge connections).

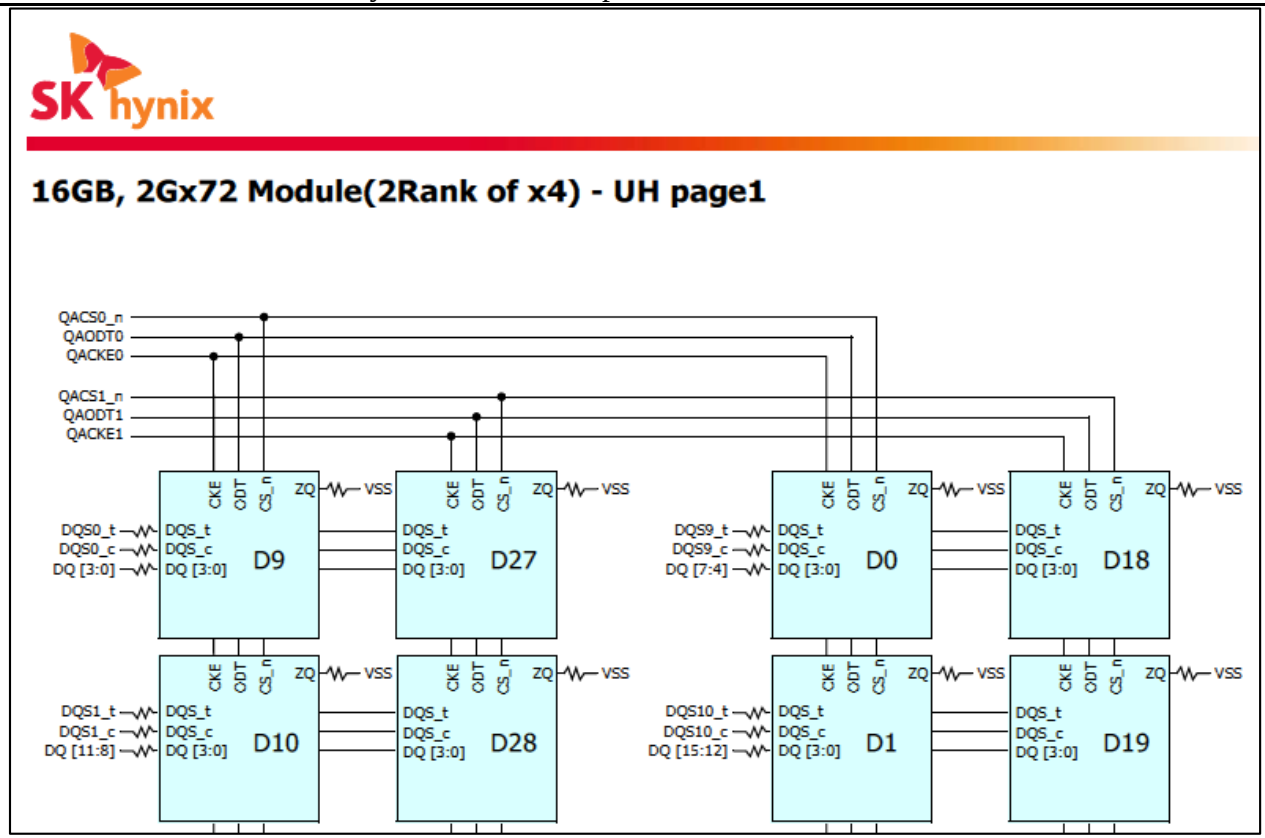
U.S. Patent No. 10,474,595: Claim 1

"dynamic random access memory elements on the printed circuit board;"

dynamic random access memory elements on the printed circuit board;	The SK hynix Products include dynamic random access memory elements on the printed circuit board. For example, the SK hynix Product includes a plurality of JEDEC-compliant synchronous dynamic random access memories ("SDRAMs").  JEDEC Standard No. 21C Page 4.20.28-5 1 Product Description This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Registered, Double Data Rate, Synchronous SDRAM Dual In-Line Memory Modules (DDR4 SDRAM RDIMMs). These DDR4 Registered DIMMs (RDIMMs) are intended for use as main memory when installed in PCs. Reference design examples are included which provide an initial basis for DDR4 RDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC4-1600, PC4-1866, PC4-2133, PC4-2400, PC4-2666, PC4-2933 and PC4-3200 support. All DDR4 RDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design. This specification follows the JEDEC standard DDR4 component specification (refer to JEDEC standard JESD79-4, at www.jedec.org). JEDEC RDIMM Standard (annotations added).

U.S. Patent No. 10,474,595: Claim 1

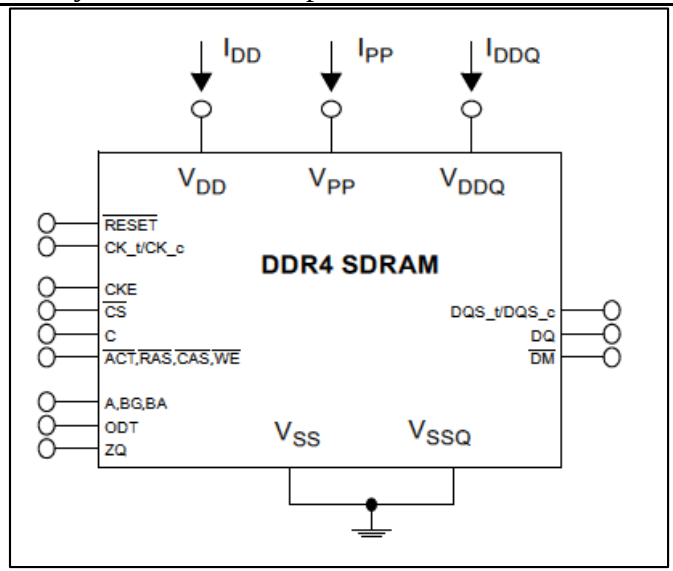
"dynamic random access memory elements on the printed circuit board;"



See SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 20 (showing SDRAM device D9, D27, D0, D18, D10, D28, D1, and D19).

U.S. Patent No. 10,474,595: Claim 1

"dynamic random access memory elements on the printed circuit board;"



See SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 55.

Specifically, the SK hynix HMA42GR7AFR4N-UHTD comprises 36 SDRAM components.

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD) (front side).

U.S. Patent No. 10,474,595: Claim 1

"dynamic random access memory elements on the printed circuit board;"

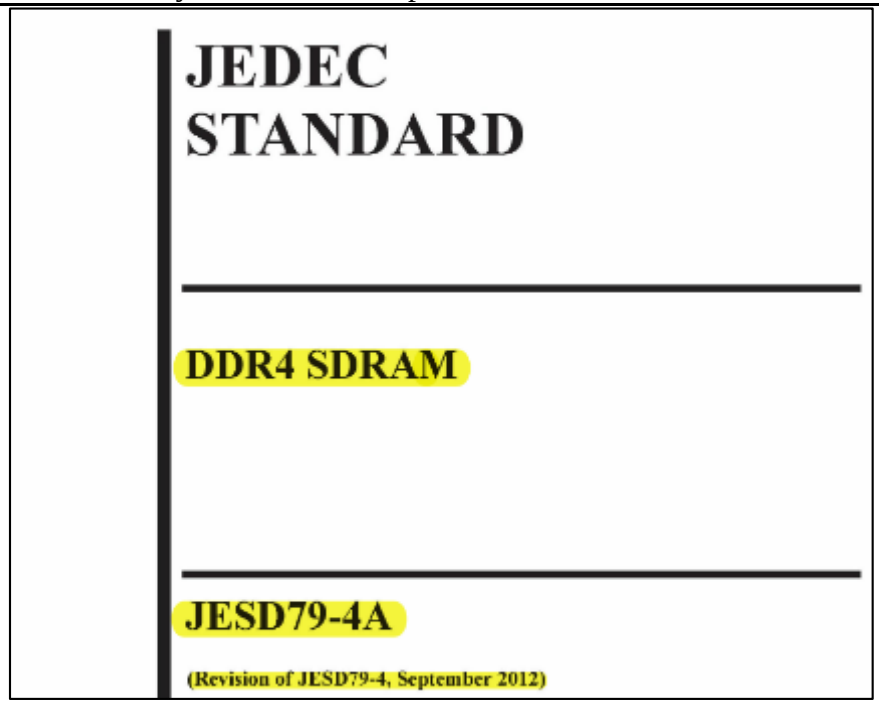
(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD) (back side).

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD) (SDRAM).

The SDRAM devices are JEDEC complaint.

U.S. Patent No. 10,474,595: Claim 1

"dynamic random access memory elements on the printed circuit board;"



JEDEC DDR4 SDRAM Specification (annotations added).
See also SKH DDR4 Device Operation at 1.

The SDRAM devices are outlined in red in the figure below.

U.S. Patent No. 10,474,595: Claim 1

"dynamic random access memory elements on the printed circuit board;"

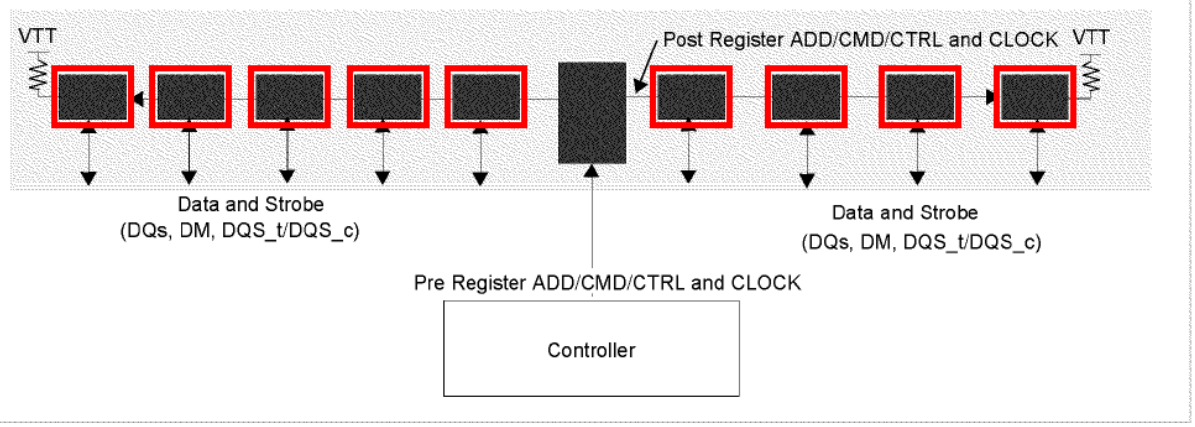
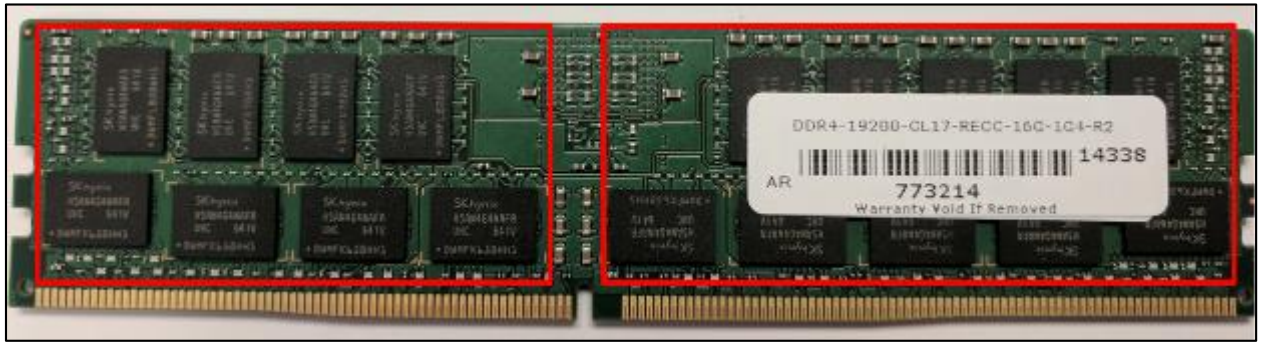


Figure 4 — Example RDIMM Topologies

JEDEC RDIMM Standard (annotations added).

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 65.

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD) (front side).



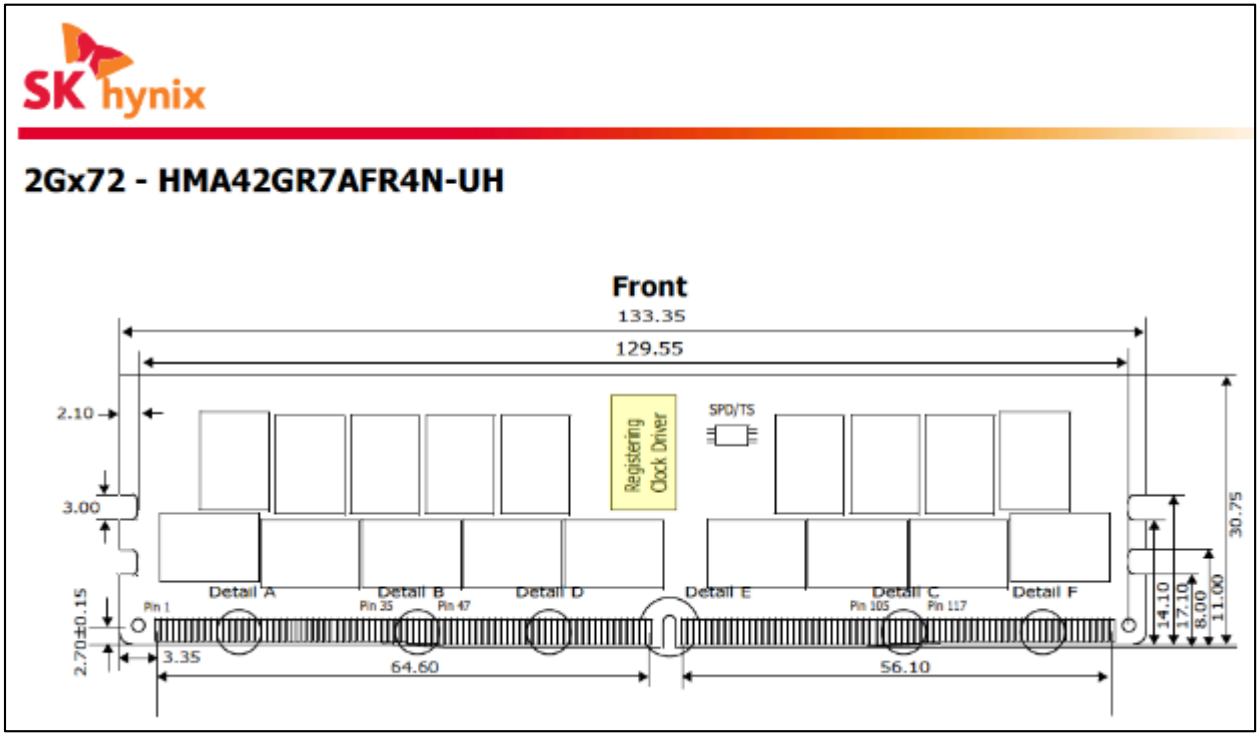
U.S. Patent No. 10,474,595: Claim 1

"dynamic random access memory elements on the printed circuit board;"

	(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD) (back side).

U.S. Patent No. 10,474,595: Claim 1

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and"

a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and	The SK hynix Products include a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection. The SK hynix Products comprise a module controller on the printed circuit board. For example, the SK hynix Products contain a JEDEC-compliant IDT 4RCD0124KC0 RCD on the printed circuit board. Some modules have lower current requirements. Any specific module must meet the SDRAM and DDR4RCD01 voltage requirements for its worst case supply currents. *See, e.g.*, JEDEC RDIMM Standard (annotation added).  SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 81 (annotations added). Specifically, the SK hynix Products contain an IDT 4RCD0124KC0 RCD.

U.S. Patent No. 10,474,595: Claim 1

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and"

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

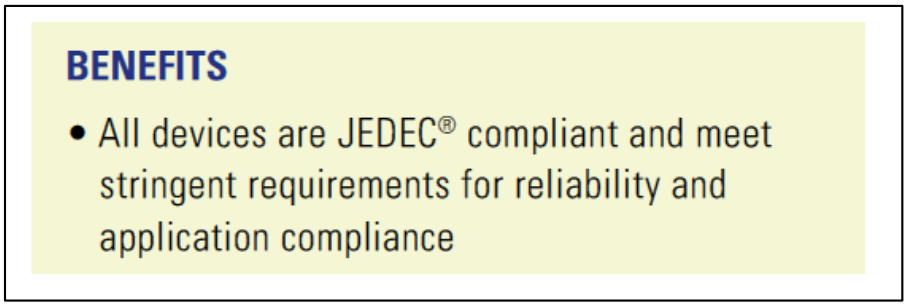
(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

The IDT 4RCD0124KC0 RCD is JEDEC Compliant.

U.S. Patent No. 10,474,595: Claim 1

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and"

See 4RCD0124K DDR4 Register Clock Driver Webpage at 1.



IDT Leader in Server Memory Chipsets at 1.

The SK hynix Products comprise a module controller coupled to the dynamic random access memory elements. For example, the IDT 4RCD0124KC0 RCD is coupled to the plurality of dynamic random access memory elements on the PCB.

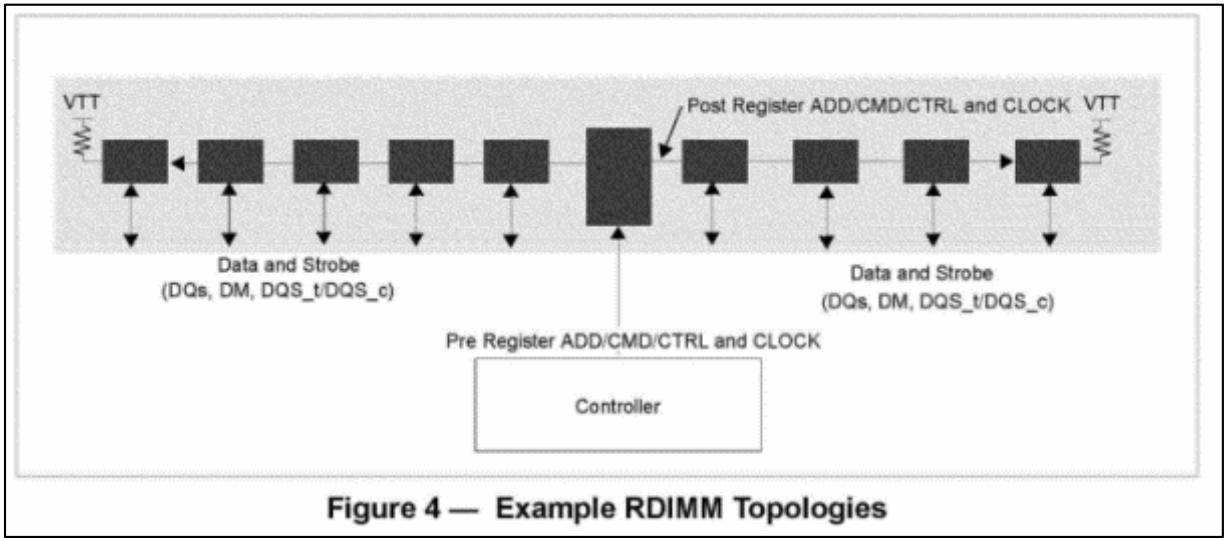


Figure 4 — Example RDIMM Topologies

JEDEC RDIMM Standard.

U.S. Patent No. 10,474,595: Claim 1

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and"

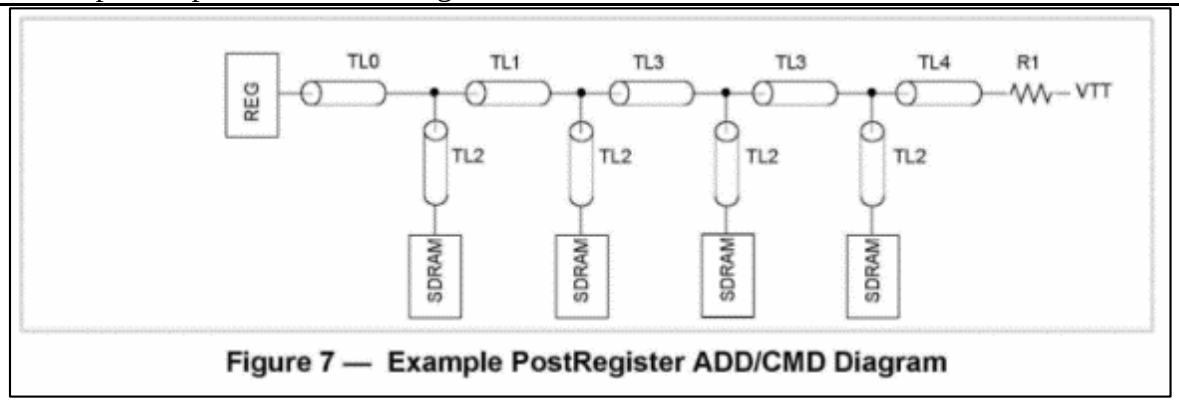
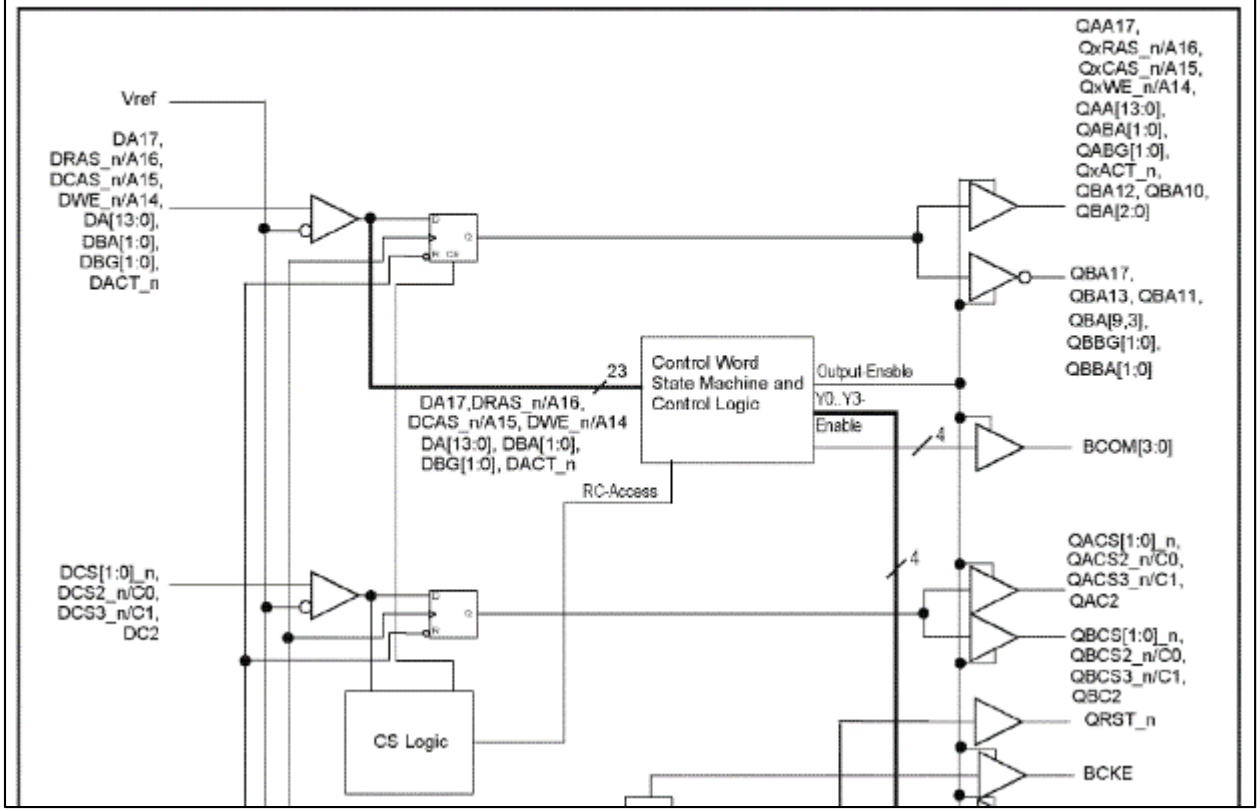


Figure 7 — Example PostRegister ADD/CMD Diagram

JEDEC RDIMM Standard.

2.17 Logic diagram



U.S. Patent No. 10,474,595: Claim 1

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and"

See JEDEC RCD01 Specification.

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1 DODT0/1	CMOS[1] V_{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DCS0_n..DCS1_n	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals.
	DCS2_n..DCS3_n or DC0..DC1	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes,. Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
	DC2	CMOS[1] V_{REF} based	DRAM corresponding register Chip ID 2 signal.
Input Address and Command bus	DA0..DA13, DA17 DBA0..DBA1, DBG0..DBG1	CMOS[1] V_{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS[1] V_{REF} based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS[1] V_{REF} based	DRAM corresponding register DACT_n signal.

See JEDEC RCD01 Specification (annotations added).

Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS[2]	Register output CKE and ODT signals.
	QACS0_n..QACS1_n, QBCS0_n..QBCS1_n	CMOS[2]	Register output Chip Select signals.
	QACS2_n..QACS3_n, QBCS2_n..QBCS3_n or QAC0..QAC1, QBC0..QBC1	CMOS[2]	Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1
	QAC2, QBC2	CMOS[2]	Register output Chip ID2 signals.

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 1

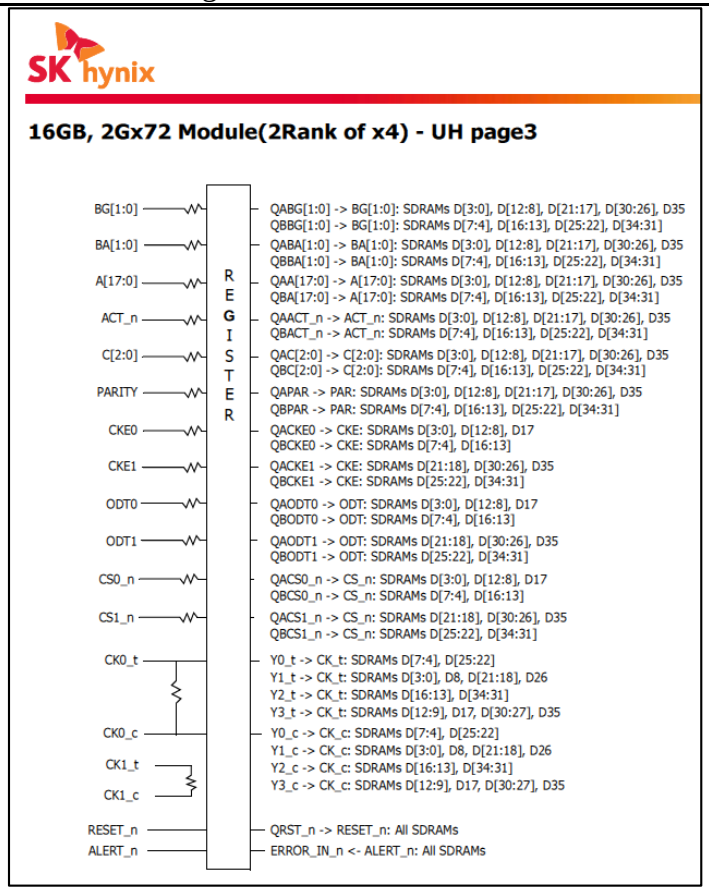
"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and"

Signal Group	Signal Name	Type	Description
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 1

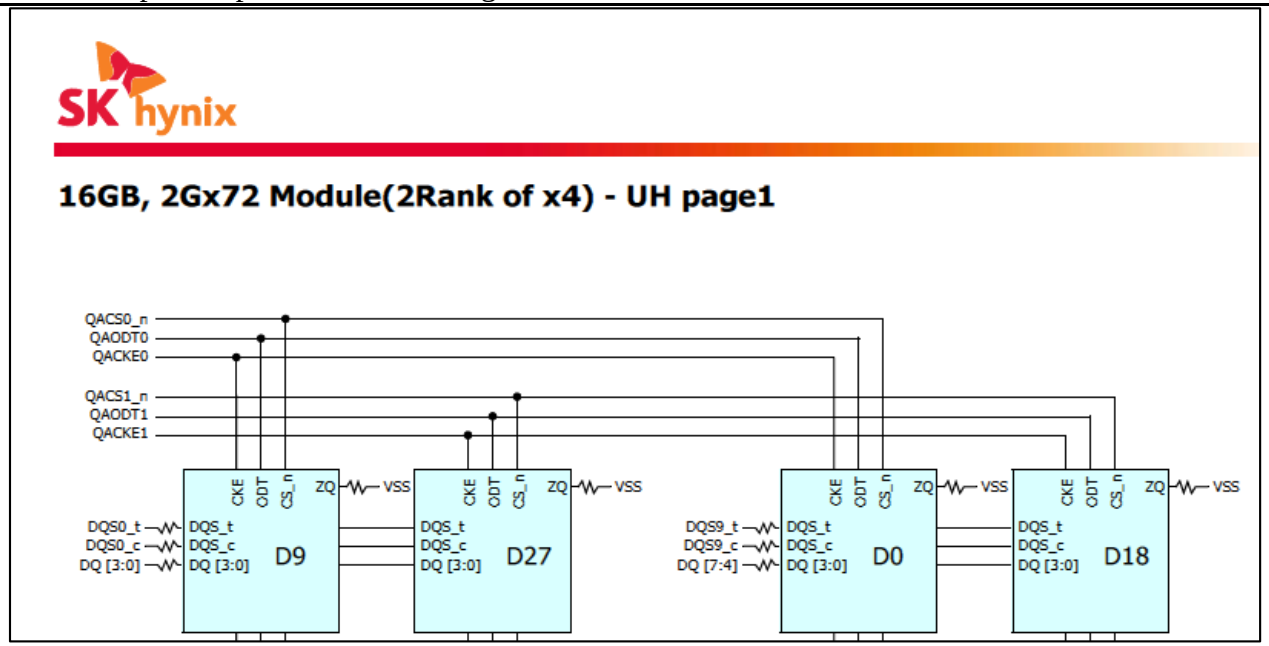
"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 22.

U.S. Patent No. 10,474,595: Claim 1

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 20.

The SK hynix Products comprise a module controller having an open drain output coupled to the error edge connection. For example, the JEDEC-complaint IDT 4RCD0124KC0 RCD contains an ALERT_n pin, which is an open drain output coupled to the error edge connection of the PCB.

U.S. Patent No. 10,474,595: Claim 1

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and"

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	$V_{DD}/2$	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS[2] differential	Redriven clock
Reset output	QRST_n	CMOS[2]	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR QBPAR	CMOS[2]	Redriven parity[3]
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
	SDA	Open drain I/O	

See JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 1

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and"

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

- CA Signals = QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2, QxPAR
- Control Signals = QxCKE0/1, QxODT0/1, QxC2, QxCS[1:0]_n for Dual CS mode, QxCS[3:0]
- CK = Yn_t - Yn_c

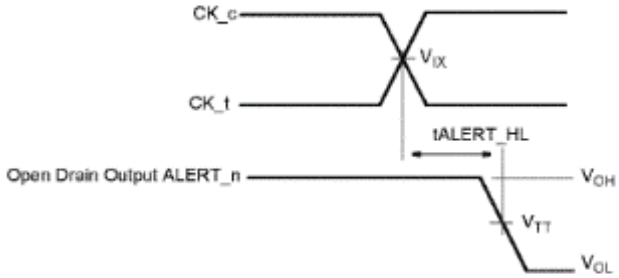


Figure 72 — Voltage waveforms, tALERT_HL Measurement

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 1

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and"

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I²C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I²C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I²C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply

JEDEC RDIMM Standard (annotation added).

ALERT_n	Output (Input)	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system.

JEDEC RDIMM Standard (annotation added).

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 5, 7.

U.S. Patent No. 10,474,595: Claim 1

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and"

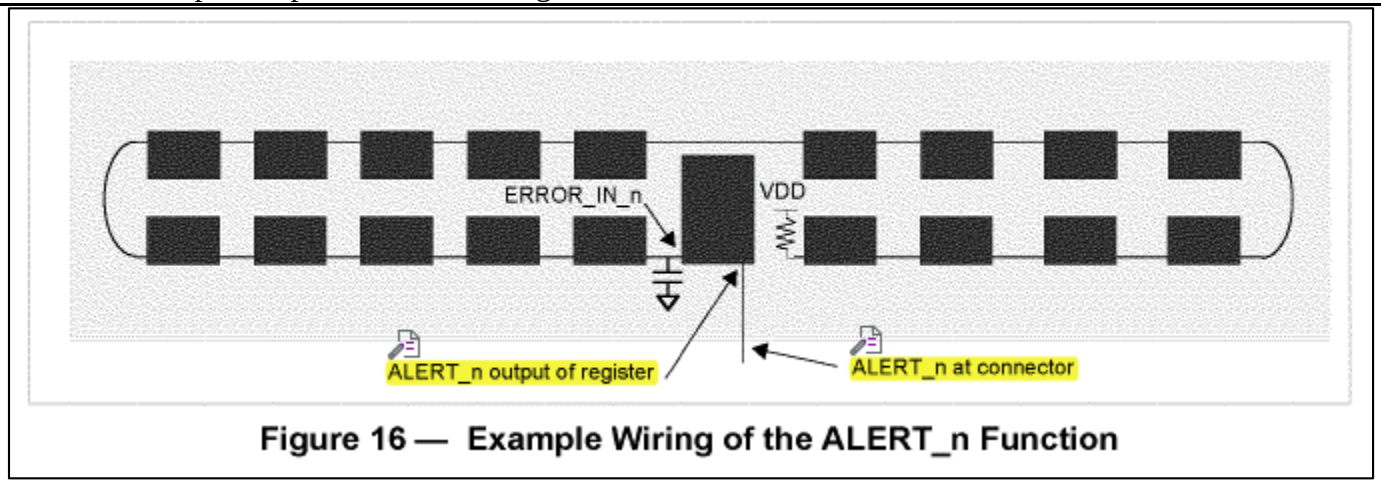
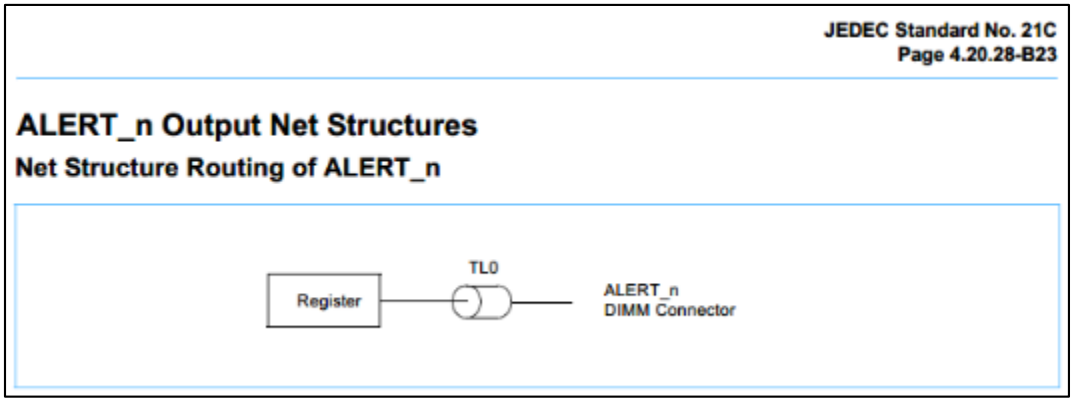


Figure 16 — Example Wiring of the ALERT_n Function

JEDEC RDIMM Standard (annotations added).



JEDEC Annex B- Raw Card B for RDIMM, at 20.

U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module is configurable to operate in any of at least a first mode and a second mode;"

wherein the memory module is configurable to operate in any of at least a first mode and a second mode;	The SK hynix Products are memory modules configurable to operate in at least a first mode and a second mode. For example, the IDT 4RCD0124KC0 RCD is configured to operate in a first mode, e.g., a normal operating mode (e.g., when RC0C control word = x000). **Table 35 — RC0C: Training Control Word** 	Setting (DA[3:0])				Definition	Encoding
---	---	---	---	---	---
x	0	0	0	Training mode selection	Normal operating mode
x	0	0	1		Clock-to-CA training mode[1]
x	0	1	0		DCS0_n loopback mode[1]
x	0	1	1		DCS1_n loopback mode[1]
x	1	0	0		DCKE0 loopback mode[1]
x	1	0	1		DCKE1 loopback mode[1]
x	1	1	0		DODT0 loopback mode[1]
x	1	1	1		DODT1 loopback mode[1]
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved | 1. In these training modes the DDR4RCD01 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals). *See* JEDEC RCD01 Specification (annotations added). For example, the IDT 4RCD0124KC0 RCD is further configured to operate in a second mode, e.g., Clock-to-CA training mode (e.g., when RC0C control word = x001). **Table 35 — RC0C: Training Control Word** | Setting (DA[3:0])				Definition	Encoding
---	---	---	---	---	---
x	0	0	0	Training mode selection	Normal operating mode
x	0	0	1		Clock-to-CA training mode[1]
x	0	1	0		DCS0_n loopback mode[1]
x	0	1	1		DCS1_n loopback mode[1]
x	1	0	0		DCKE0 loopback mode[1]
x	1	0	1		DCKE1 loopback mode[1]
x	1	1	0		DODT0 loopback mode[1]
x	1	1	1		DODT1 loopback mode[1]
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved	 1. In these training modes the DDR4RCD01 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals). *See* JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module is configurable to operate in any of at least a first mode and a second mode;"

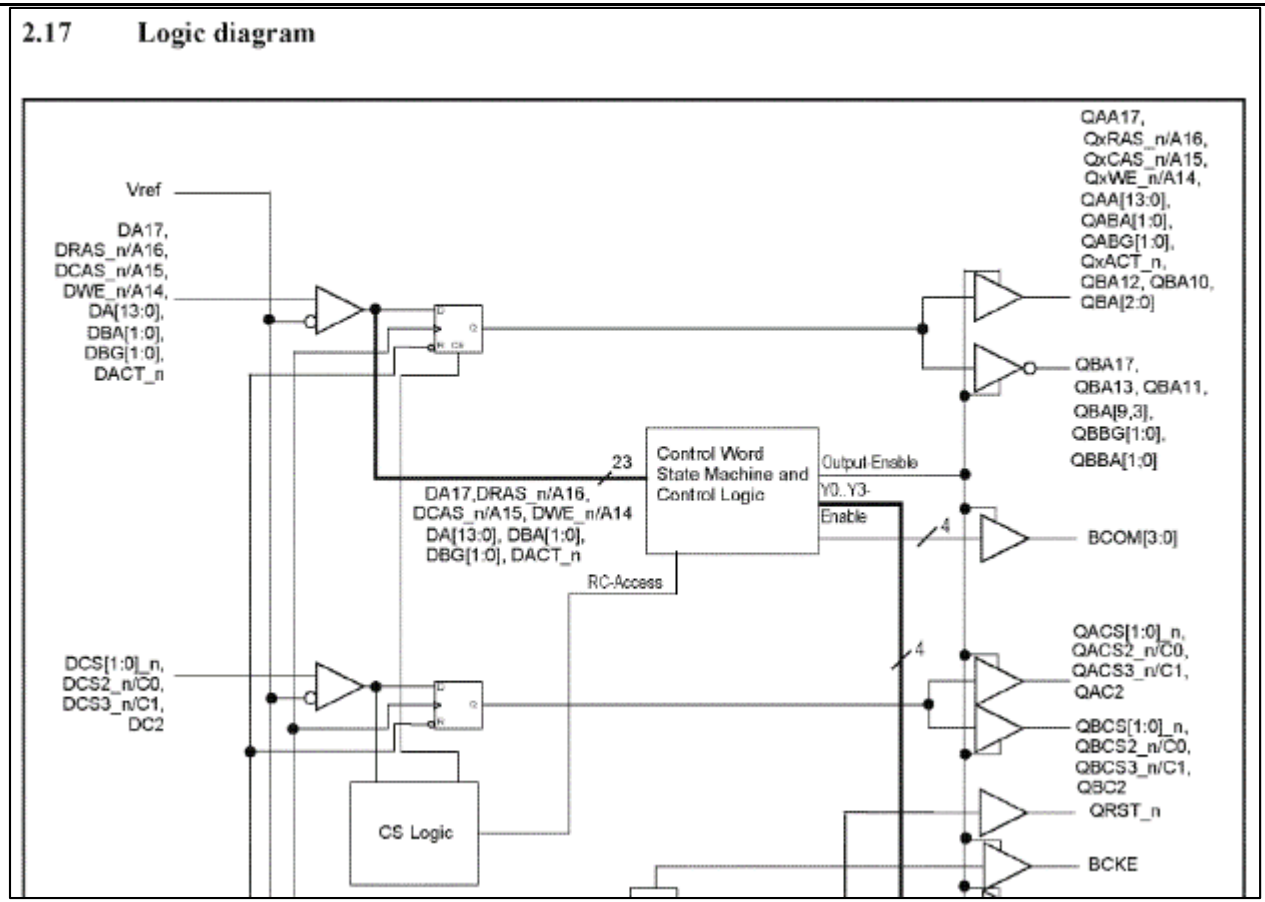
U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;	In the first mode, the SK hynix Products are configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections. For example, the SK hynix Products are configured to operate in a normal operating mode, e.g., a first mode. **Table 35 — RC0C: Training Control Word** | Setting (DA[3:0])				Definition	Encoding
---	---	---	---	---	---
x	0	0	0	Training mode selection	Normal operating mode
x	0	0	1		Clock-to-CA training mode[1]
x	0	1	0		DCS0_n loopback mode[1]
x	0	1	1		DCS1_n loopback mode[1]
x	1	0	0		DCKE0 loopback mode[1]
x	1	0	1		DCKE1 loopback mode[1]
x	1	1	0		DODT0 loopback mode[1]
x	1	1	1		DODT1 loopback mode[1]
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved	 1. In these training modes the DDR4RCD01 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals). *See* JEDEC RCD01 Specification (annotations added). The SK hynix Products are configured to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections. For example, during the first mode (e.g., a normal mode of operation), the RCD receives address and control signals corresponding to read and write commands from the memory controller via the second edge connections. The RCD outputs corresponding address and control signals to the SDRAM devices, which cause the SDRAM devices to execute read and write operations.

U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"



See JEDEC RCD01 Specification.

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1 DODT0/1	CMOS[1] V_{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DCS0_n..DCS1_n	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals.
	DCS2_n..DCS3_n or DC0..DC1	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes,. Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
	DC2	CMOS[1] V_{REF} based	DRAM corresponding register Chip ID 2 signal.
Input Address and Command bus	DA0..DA13, DA17 DBA0..DBA1, DBG0..DBG1	CMOS[1] V_{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS[1] V_{REF} based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS[1] V_{REF} based	DRAM corresponding register DACT_n signal.

See JEDEC RCD01 Specification (annotations added).

Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS[2]	Register output CKE and ODT signals.
	QACS0_n..QACS1_n, QBCS0_n..QBCS1_n	CMOS[2]	Register output Chip Select signals.
	QACS2_n..QACS3_n, QBCS2_n..QBCS3_n or QAC0..QAC1, QBC0..QBC1	CMOS[2]	Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1
	QAC2, QBC2	CMOS[2]	Register output Chip ID2 signals.

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 1

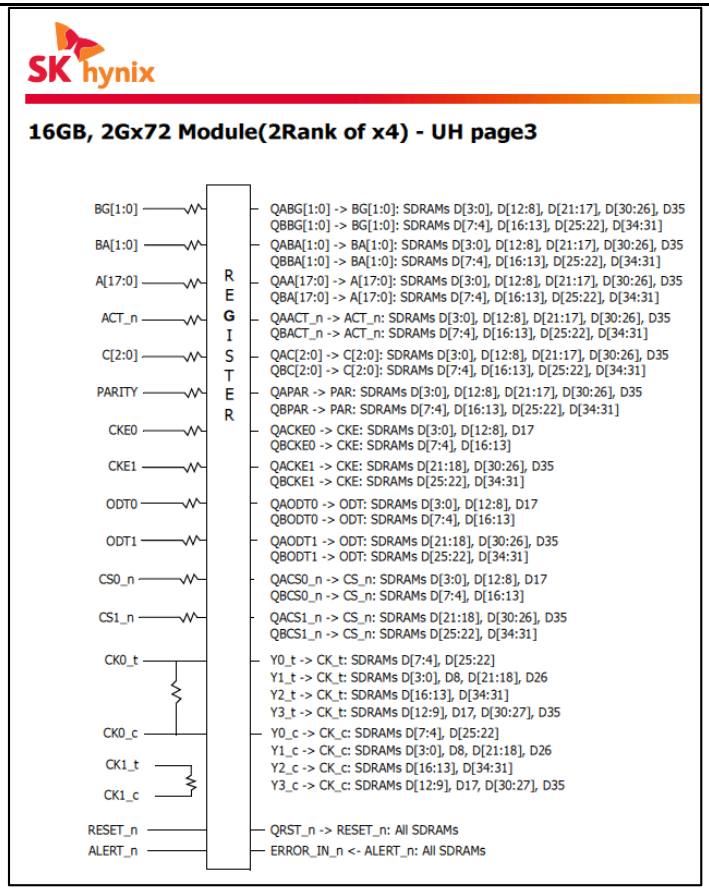
"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

Signal Group	Signal Name	Type	Description
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 1

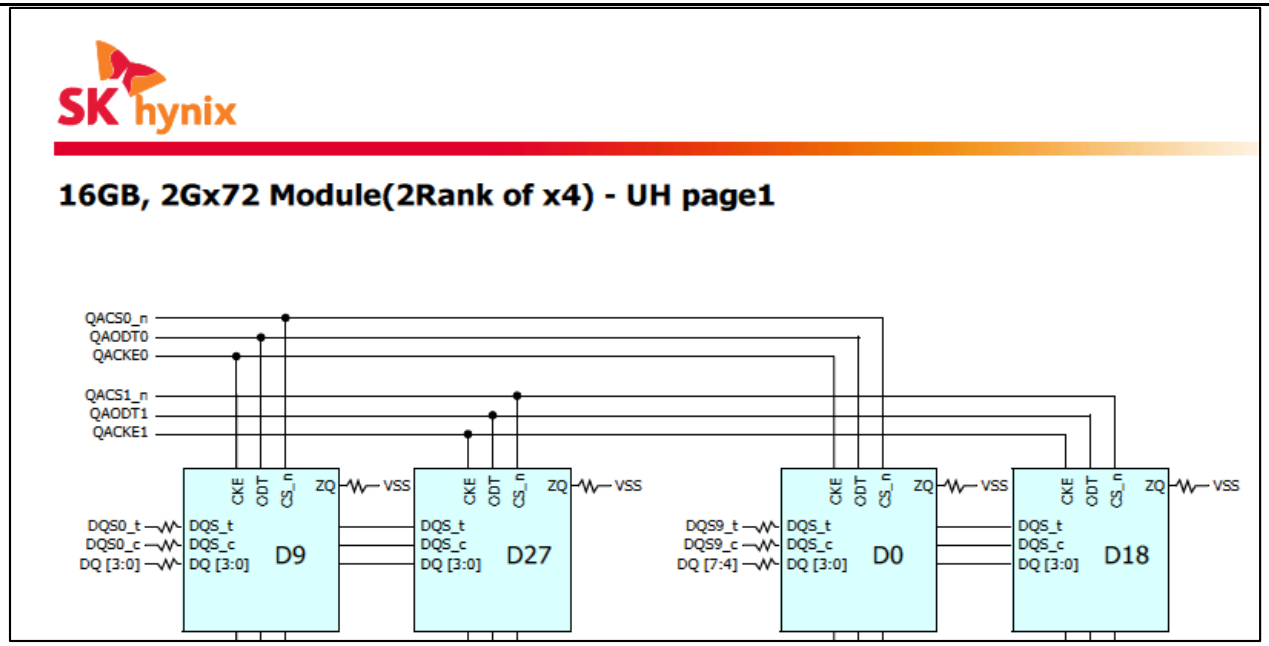
"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 22.

U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 20.

The SDRAM components receive these signals as inputs from the RCD.

U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

2.6 Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code

JEDEC DDR4 SDRAM Specification.

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 6.

RAS_n/A16, CAS_n/ A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table

JEDEC DDR4 SDRAM Specification.

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 6.

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.

JEDEC DDR4 SDRAM Specification.

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 6.

These signals are used during reads and writes that occur during operational mode, e.g., the first mode.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner.

JEDEC DDR4 SDRAM Specification (annotations added).
See also SKH DDR4 Device Operation at 7.

4.22 ACTIVATE Command

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BG0-BG1 in X4/8 and BG0 in X16 select the bankgroup; BA0-BA1 inputs selects the bank within the bankgroup, and the address provided on inputs A0-A17 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank or a precharge all command is issued. A bank must be precharged before opening a different row in the same bank.

JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 94.

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

Additionally, the RCD outputs chips select commands QACS0_n, QACS1_N, and/or QACS3_n, and QBCS0_n, QBCS1_N, and/or QBCS3_n, which activate the relevant SDRAM chip depending on the mode of operation.

2.2 Features and Functions

The DDR4RCD01 has three basic modes of operation associated with the DA[1:0] bits in the DIMM Configuration Control Word (RC0D):

- In **Direct DualCS mode** (DA[1:0] = 00) the component has two chip select inputs, DCS0_n and DCS1_n, and two copies of each chip select output, QACS0_n, QACS1_n, QBCS0_n and QBCS1_n. The inputs pins DC[2:0] are forwarded to two sets of output pins, QAC[2:0] and QBC[2:0]. This is the normal operating mode ("QuadCS disabled" and "Encoded CS disabled").
- In **Direct QuadCS mode** (DA[1:0] = 01), the component has four chip select inputs, the two dedicated inputs DCS[1:0]_n and the DC[0] input pin functioning as DCS2_n and the DC[1] input pin functioning as DCS3_n, and two copies of each chip select output, QACS[3:0]_n and QBCS[3:0]_n. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "QuadCS enabled" mode.

  In the two modes above the DDR4 register does not need to decode input signals to generate any chip select outputs.
- In **Encoded QuadCS mode** (DA[1:0] = 11), two copies of four output chip selects, i.e., QACS[3:0]_n and QBCS[3:0]_n, are decoded out of two DCS[1:0]_n inputs and the DC[0] input. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "Encoded QuadCS" mode.

See JEDEC RCD01 Specification.

In response to the address and command information received via the second edge connections, the SK hynix Products communicate data signals via the first edge connections while performing memory read or write operations. For example the DQ and DQS signals (first edge connections) are used to communicate data signals between the memory module and host in response to read/write commands and addressing information received from the second edge connections:

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I^2C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I^2C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I^2C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS9_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	DM0_n-DM8_n	Data Mask
DQS0_c-DQS17_c	Data Buffer data strobes	RESET_n	Set Register and SDRAMs to a Known State

DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.

DQS0_t-DQS17_t, DQS0_c-DQS17_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

JEDEC RDIMM Standard.

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 5, 7.

U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

6 DIMM Design Details

6.1 Signal Groups

This specification categorizes DDR4 SDRAM signals into six groups. Figure 4 illustrates the DIMM wiring. All signal groups, except DQ, implement a fly-by topology.

The signal groups are:

1. DQ and DQS signals connector to SDRAM

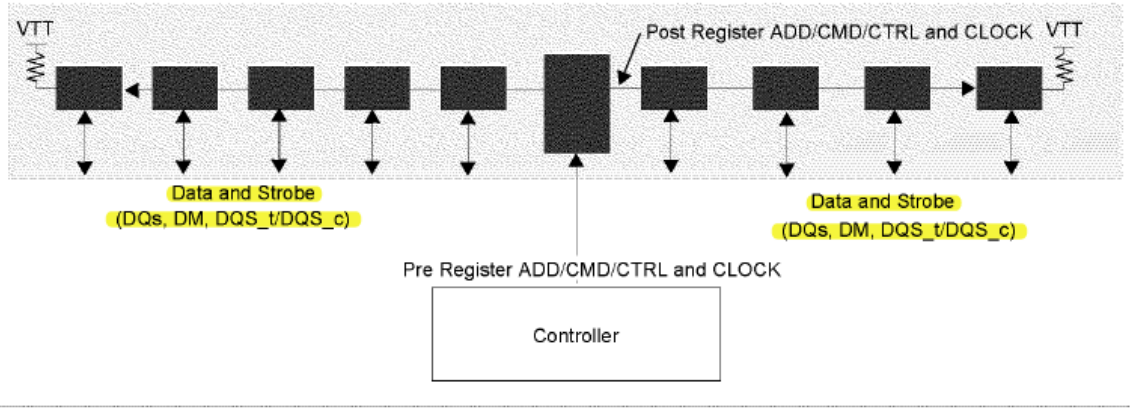


Figure 4 — Example RDIMM Topologies

JEDEC RDIMM Standard (annotations added).

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

JEDEC DDR4 SDRAM Specification (annotations added).
See also SKH DDR4 Device Operation at 7.

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

JEDEC DDR4 SDRAM Specification (annotations added).

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 7.

U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

JEDEC Standard No. 79-4A
Page 86

4.24.1.2 READ Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 67 and is applied when the DLL is enabled and locked.

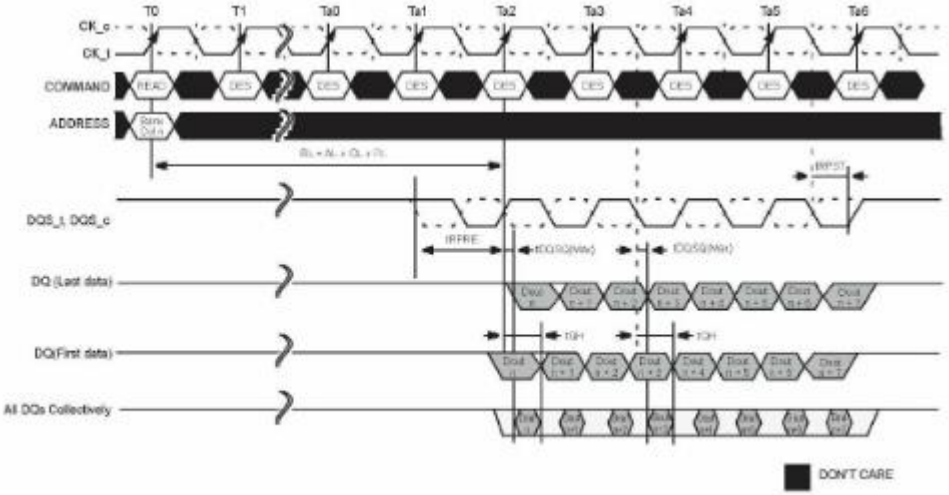
Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

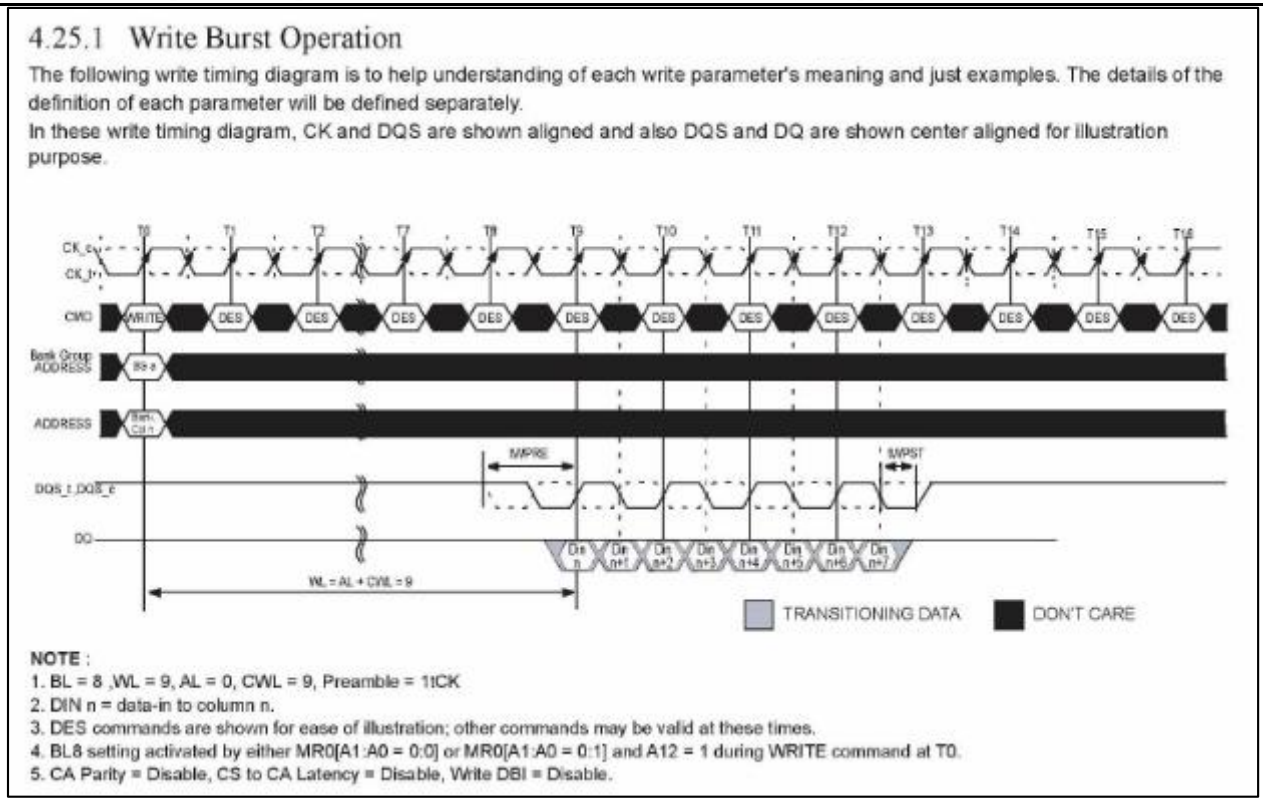
tDQSQ: both rising/falling edges of DQS, no tAC defined.



See, e.g., JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 97.

U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"



See, e.g., JEDEC DDR4 SDRAM Specification.
See also JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 126, 94-144.

In the second mode, the SK hynix Products are not accessed by the memory controller for normal memory read or write operations, and are configurable to perform operations related to one or more training sequences.

For example, while the SK hynix Product is in Clock-to-CA training mode (e.g., a second mode), the dynamic random access memory devices (DRAMs) of the memory module are isolated from normal use, and normal operational read/write commands are not decoded.

U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

	The DRAM is protected by driving the RCD control outputs at inactive levels. The RCD may either force all outputs than can be chip selects (including QxC0/CS2_n and QxC1/CS3_n) HIGH and all QxCKE and QxODT outputs LOW OR hold the previous values on QxCA/QxCS/QxCKE/QxODT before entering any of the CA training modes. The data buffer is protected by driving the buffer control interface signals at inactive levels. The RCD may either drive BODT and BCKE outputs LOW and BCOM[3:0] to '1010' (NOP command) OR the RCD may hold the previous values on BODT/BCKE/BCOM before entering any of the CA training modes. The RCD does not decode commands while any RC0C training mode is enabled. It is thus necessary for the register to correspondingly disable and ignore unused inputs in each training mode. The following two methods to change or exit CA training modes are supported: (a) Write access to RC0C through I^2C Bus and (b) DRST_n Reset event. *See* JEDEC RCD01 Specification. Further, while in the second mode, the SK hynix Products are configurable to perform operations related to one or more training sequences.

U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

2.12 CA Bus Training Modes

The DDR4RCD01 supports several training modes (selected in Table 35, "RC0C: Training Control Word") in order to assist the memory controller in aligning the incoming command/address and control signals optimally to the input clock signal CK_t/CK_t. These training modes are only available if a non-zero latency adder has been selected.

In Clock-to-CA training mode the DDR4RCD01 ORs all enabled Dn inputs[1] every other cycle together and loops back the result to the ALERT_n output pin. In this mode, the DPAR input is sampled at the same time as the other Dn inputs. The ALERT_n latency relative to the DQn inputs is the same 3 cycles as in the normal parity mode. During any of the CA bus training modes, QCA/QxCKEn and QxODTn hold their previous values and parity checking is disabled.

The memory controller can use the Clock-to-CA training mode and feedback from the DDR4RCD01 to adjust the CK_t-CK_c to Dn relationship analogous to the write leveling sequence which adjusts the DQS-DQS_n to CK_t-CK_c relationship. The memory controller writes consecutive sequences of all '1's and all '0's on the CA bus and pulls in the Dn timing until the DDR4RCD01 samples all Dn inputs as 0, which is indicated with the LOW assertion of ALERT_n. This position indicates the start position of a cumulative CA bus "eye opening". The memory controller advances the clock position or pulls in the Dn timing until the DDR4RCD01 samples at least one input as '1', which is indicated by ALERT_n remaining high three cycles after the last command. This position indicates the end position of a cumulative CA bus "eye opening". The memory controller can now position either the clock phase or the Dn input timing so that the clock edge is in the middle of this "eye opening" to achieve equal amounts of setup and hold time relative to the clock edge.

Figure 22 shows three sampling phase positions where the loopback ALERT_n pin transmits either a consistent 0 output, a randomly toggling 1/0 output or a consistent 1 output, indicating sampling positions at the LOW time, the transition time or the HIGH time of the inputs, respectively.

The memory controller can use the DCS0_n, DCS1_n, DCKE0, DCKE1, DODT0 and DODT0 loop back modes in similar fashion. In each of these modes a single input signal is looped back to the ALERT_n output and the memory controller can determine the optimal clock position for each of the control signals that are used for a particular DIMM. Once the optimal clock position for all CMD/ADDR and control inputs has been established, the memory controller can determine the best clock position for the whole set of input signals or potentially move the timing of individual control signals around to increase either setup or hold margins relative to the clock edge.

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 1

"wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;"

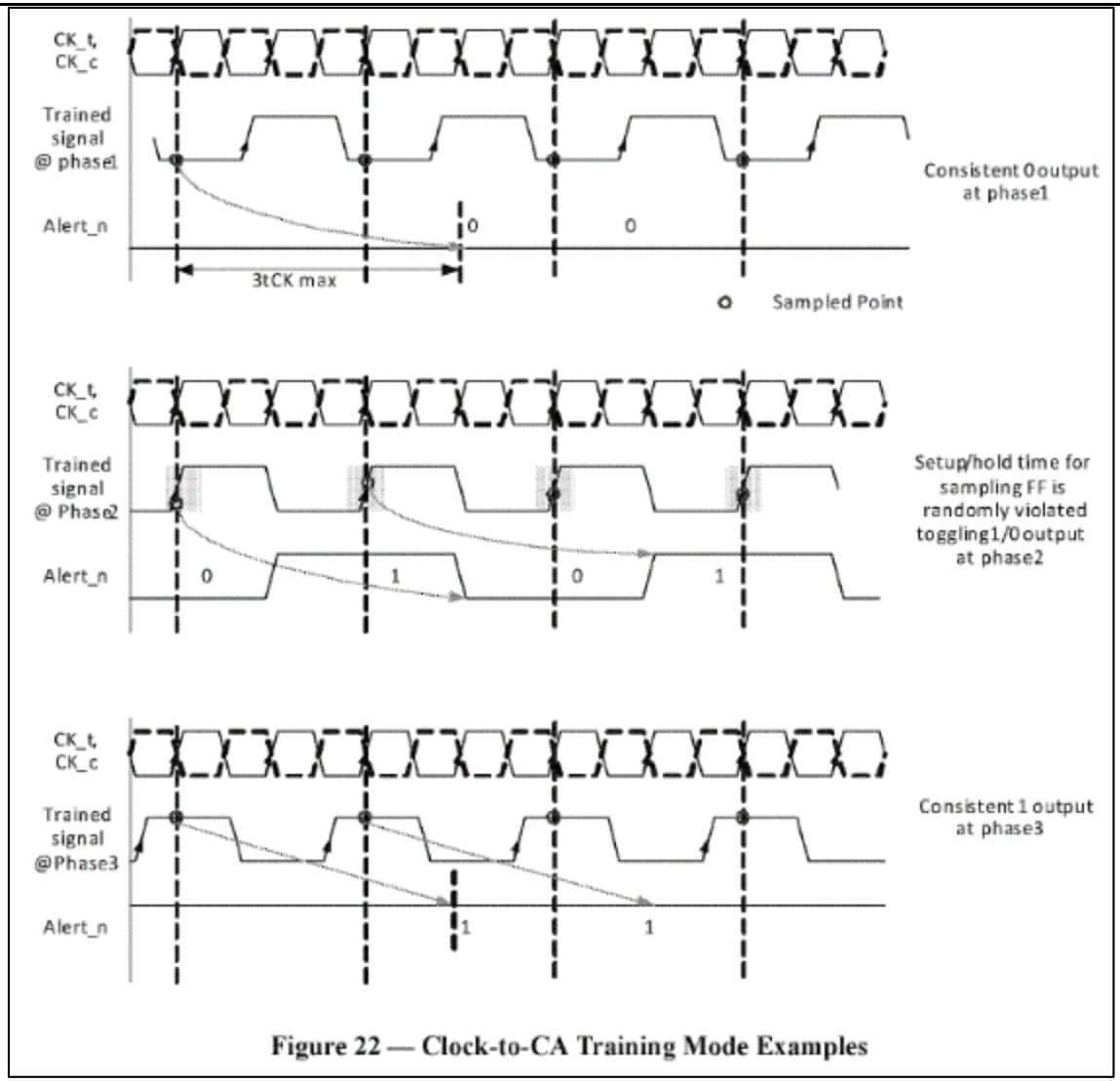


Figure 22 — Clock-to-CA Training Mode Examples

See JEDEC RCD01 Specification.

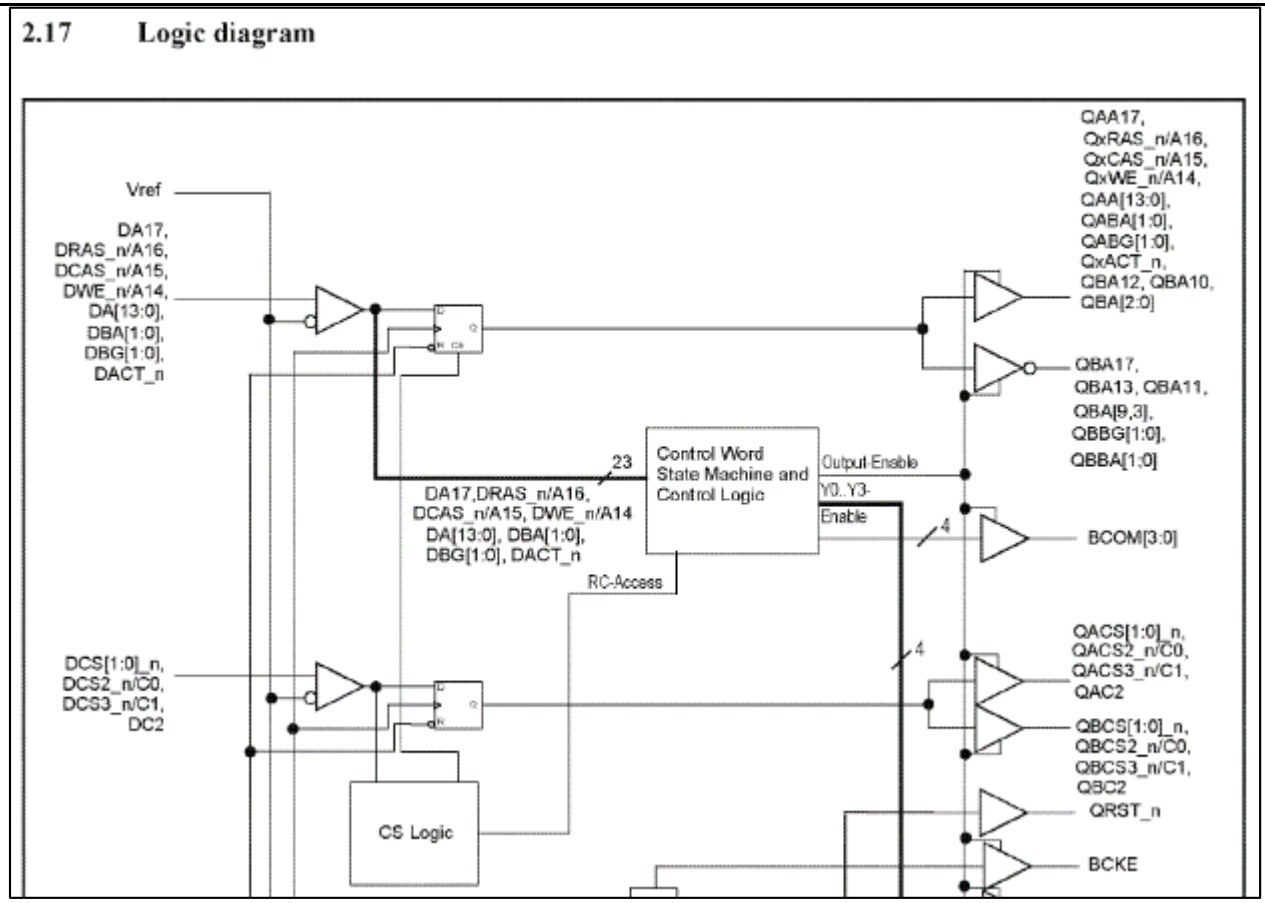
U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;	The module controller of the SK hynix Products is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements of the SK hynix Products are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller of the SK hynix Products is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the SK hynix Products are in the first mode. While the SK hynix Products are in the first mode, the module controller of the SK hynix Products is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations. For example, during the first mode (e.g., a normal mode of operation), the RCD receives address and control signals corresponding to read and write commands from the memory controller via the second edge connections.

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"



See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1 DODT0/1	CMOS[1] V_{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DCS0_n..DCS1_n	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals.
	DCS2_n..DCS3_n or DC0..DC1	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes,. Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
	DC2	CMOS[1] V_{REF} based	DRAM corresponding register Chip ID 2 signal.
Input Address and Command bus	DA0..DA13, DA17 DBA0..DBA1, DBG0..DBG1	CMOS[1] V_{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS[1] V_{REF} based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS[1] V_{REF} based	DRAM corresponding register DACT_n signal.

See JEDEC RCD01 Specification (annotations added).

Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS[2]	Register output CKE and ODT signals.
	QACS0_n..QACS1_n, QBCS0_n..QBCS1_n	CMOS[2]	Register output Chip Select signals.
	QACS2_n..QACS3_n, QBCS2_n..QBCS3_n or QAC0..QAC1, QBC0..QBC1	CMOS[2]	Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1
	QAC2, QBC2	CMOS[2]	Register output Chip ID2 signals.

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 1

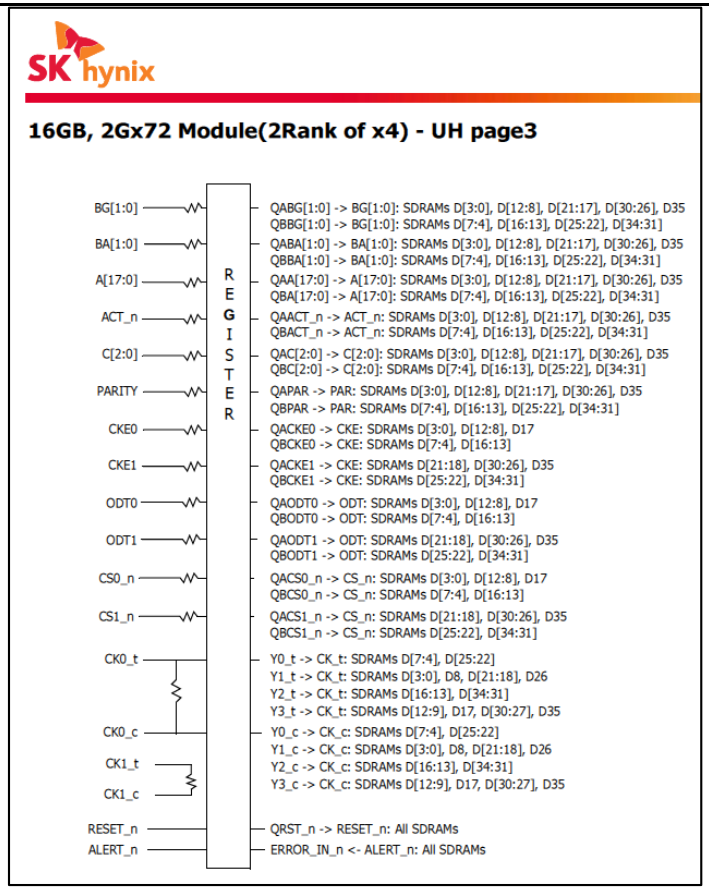
"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

Signal Group	Signal Name	Type	Description
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 1

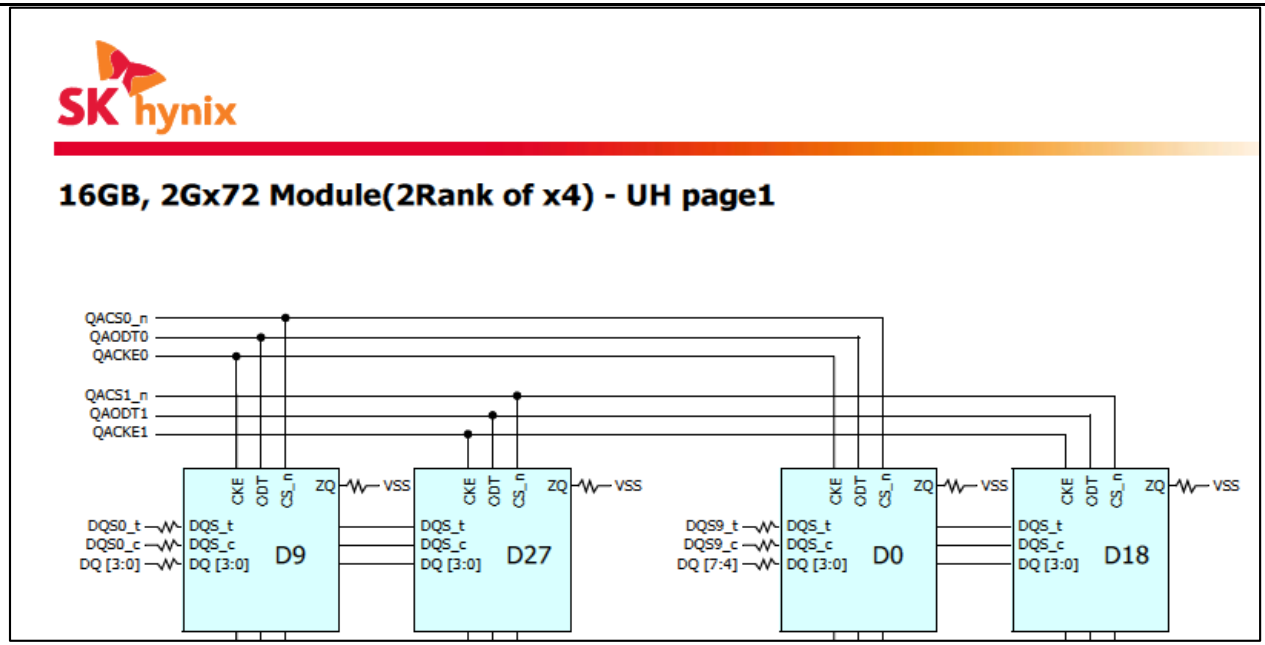
"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 22.

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 20.

Further, in the first mode, the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals. For example, the RCD outputs the address and control signals to the SDRAM devices, which cause the SDRAM devices to execute read and write operations. The SDRAM components receive these signals as inputs from the RCD.

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

2.6 Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code

JEDEC DDR4 SDRAM Specification.

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 6.

RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table

JEDEC DDR4 SDRAM Specification.

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 6.

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.

JEDEC DDR4 SDRAM Specification.

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 6.

These signals are used during reads and writes that occur during the normal operational mode, e.g., the first mode.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner.

JEDEC DDR4 SDRAM Specification (annotations added).
See also SKH DDR4 Device Operation at 7.

4.22 ACTIVATE Command

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BG0-BG1 in X4/8 and BG0 in X16 select the bankgroup; BA0-BA1 inputs selects the bank within the bankgroup, and the address provided on inputs A0-A17 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank or a precharge all command is issued. A bank must be precharged before opening a different row in the same bank.

JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 94.

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

Additionally, the RCD outputs chips select commands QACS0_n, QACS1_N, and/or QACS3_n, and QBCS0_n, QBCS1_N, and/or QBCS3_n, which activate the relevant SDRAM chip depending on the mode of operation.

2.2 Features and Functions

The DDR4RCD01 has three basic modes of operation associated with the DA[1:0] bits in the DIMM Configuration Control Word (RC0D):

- In **Direct DualCS mode** (DA[1:0] = 00) the component has two chip select inputs, DCS0_n and DCS1_n, and two copies of each chip select output, QACS0_n, QACS1_n, QBCS0_n and QBCS1_n. The inputs pins DC[2:0] are forwarded to two sets of output pins, QAC[2:0] and QBC[2:0]. This is the normal operating mode ("QuadCS disabled" and "Encoded CS disabled").
- In **Direct QuadCS mode** (DA[1:0] = 01), the component has four chip select inputs, the two dedicated inputs DCS[1:0]_n and the DC[0] input pin functioning as DCS2_n and the DC[1] input pin functioning as DCS3_n, and two copies of each chip select output, QACS[3:0]_n and QBCS[3:0]_n. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "QuadCS enabled" mode.

  In the two modes above the DDR4 register does not need to decode input signals to generate any chip select outputs.
- In **Encoded QuadCS mode** (DA[1:0] = 11), two copies of four output chip selects, i.e., QACS[3:0]_n and QBCS[3:0]_n, are decoded out of two DCS[1:0]_n inputs and the DC[0] input. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "Encoded QuadCS" mode.

See JEDEC RCD01 Specification.

In accordance with those address and control signals, the SDRAM communicate data signals with the memory controller via the first edge connections. For example the DQ and DQS signals (first edge connections) are used to communicate data signals between the memory module and host in response to read/write commands and addressing information received from the second edge connections:

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I^2C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I^2C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I^2C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS9_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	DM0_n-DM8_n	Data Mask
DQS0_c-DQS17_c	Data Buffer data strobes	RESET_n	Set Register and SDRAMs to a Known State

DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.

DQS0_t-DQS17_t, DQS0_c-DQS17_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

JEDEC RDIMM Standard.

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 5, 7.

6 DIMM Design Details

6.1 Signal Groups

This specification categorizes DDR4 SDRAM signals into six groups. Figure 4 illustrates the DIMM wiring. All signal groups, except DQ, implement a fly-by topology.

The signal groups are:

1. DQ and DQS signals connector to SDRAM

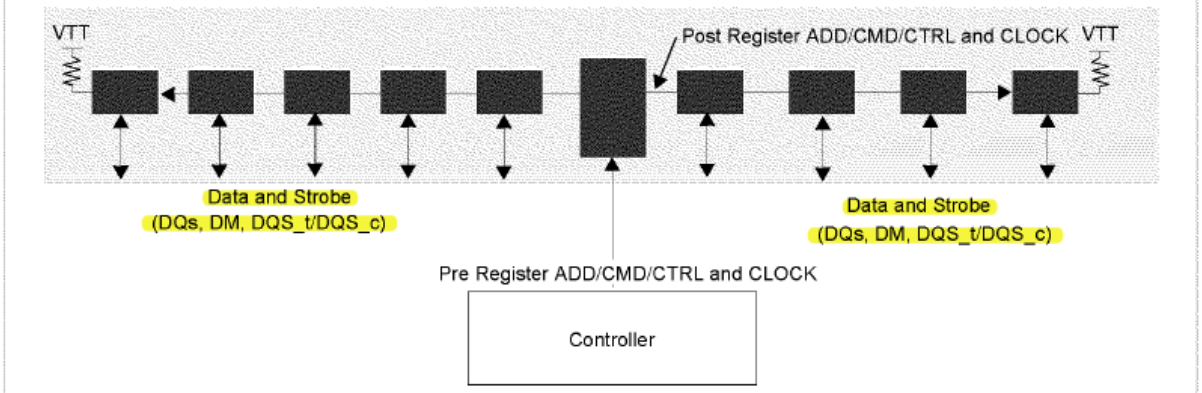


Figure 4 — Example RDIMM Topologies

JEDEC RDIMM Standard (annotations added).

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

	Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register. JEDEC DDR4 SDRAM Specification (annotations added). *See also* SKH DDR4 Device Operation at 7. **Symbol** | **Type** | **Function** DQ | Input / Output | Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used. DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c | Input / Output | Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended. JEDEC DDR4 SDRAM Specification (annotations added). *See also* SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 7.

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

JEDEC Standard No. 79-4A
Page 86

4.24.1.2 READ Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 67 and is applied when the DLL is enabled and locked.

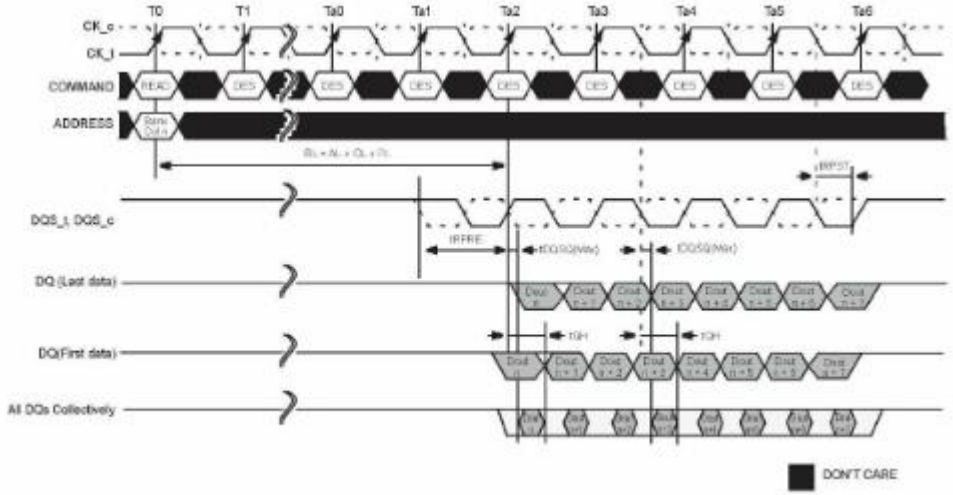
Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

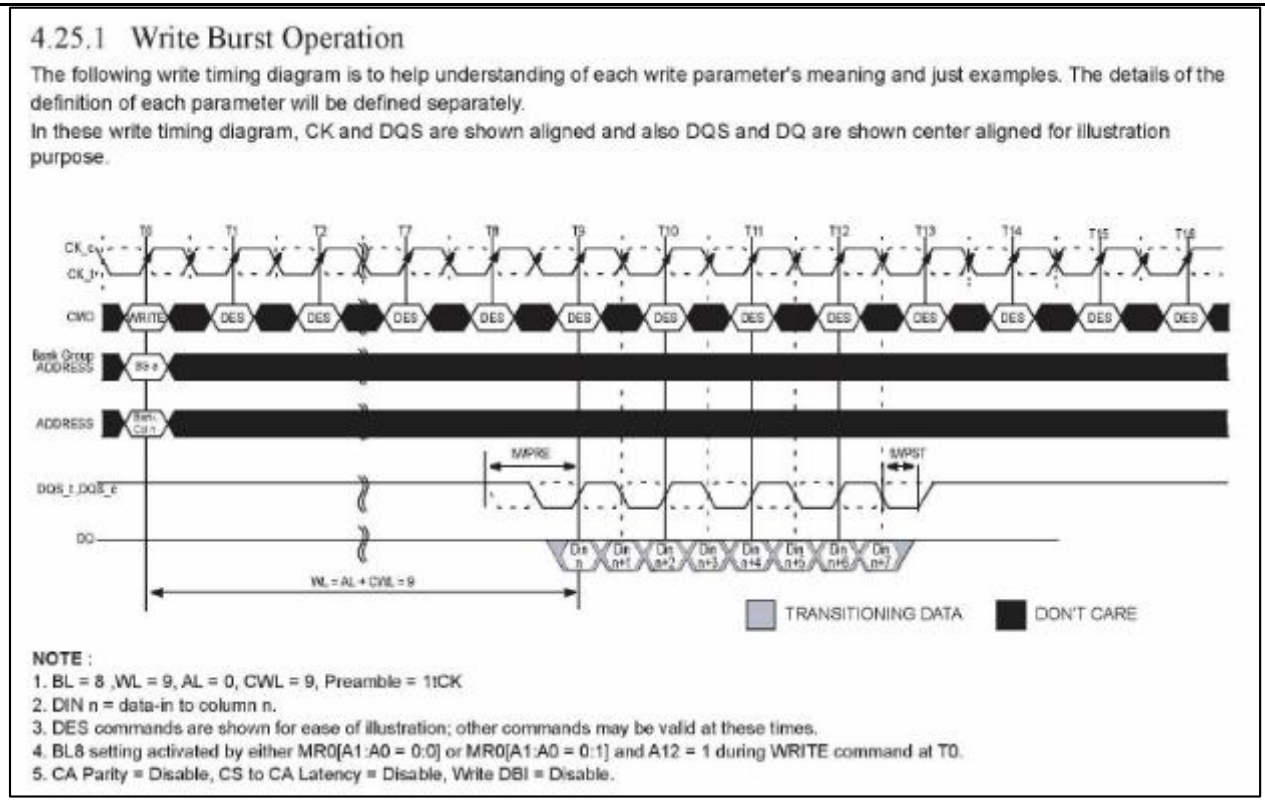
tDQSQ: both rising/falling edges of DQS, no tAC defined.



See, e.g., JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 97.

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"



See, e.g., JEDEC DDR4 SDRAM Specification.
See also JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 126, 94-144.

The module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the SK hynix Products are in the first mode. For example, the ALERT_n pin of the SK hynix Products is used to indicate a parity error while the memory module operates in the first mode (e.g., a normal mode of operation).

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I^2C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I^2C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I^2C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply

JEDEC RDIMM Standard (annotation added).

ALERT_n	Output (Input)	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system.

JEDEC RDIMM Standard (annotation added).

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 5, 7.

During the first mode (e.g., a normal mode of operation), the RCD uses the ALERT_n signal to indicate a parity error having occurred.

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

	After the DDR4RCD01 receives DPAR from the memory controller, it compares it with the data received on the CA inputs and indicates on its open-drain ALERT_n pin (active LOW) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[n:0]_n signals being LOW. The convention of parity is even parity, i.e., valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even. The DIMM-dependent control signals (DCKE0, DCKE1, DCS0_n .. DCS3_n, DODT0 and DODT1) are not included in the parity check computations. Even after a CA parity error has been registered, the device will still forward DCKEn and DODTn to the DRAMs, and the device will enter CKE power down mode depending on the DCKEn transitions. If a parity error occurs and parity checking is enabled in RC0E, the DDR4 register sets the 'CA Parity Error Status' bit in RCFx to '1'and disables parity checking. ALERT_n is asserted three input clocks after the erroneous command is registered. If the 'CA Parity Error Status' bit is '0', the DDR4 register logs the error by storing the erroneous command and address bits in the Error Log Register. ALERT_n stays asserted LOW until a 'Clear CA Parity Error Status' command is sent if the 'ALERT_n Assertion' bit in the Parity Control Word (RC0E) is '0'. In this case the erroneous command and all subsequent commands *See, e.g.*, JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;"

2.18 Control Words

The device features a set of control words, which allow the optimization of the device properties for different raw card designs. DDR4RCD01 control word (RCW) writes appear like DRAM MRS commands to MR7 which are ignored by the DDR4 DRAM. Each RCW write generates an MRS command to the rank 0 DRAMs behind the register, unless there is a parity error when parity checking is enabled, in which case both the RCW write as well as the MRS command to the DRAM are blocked. The different control words and settings are described below. Any change to these control words require some time for the device to settle. For changes to the control word setting, except for RC02 (DA3) and RC0A/RC3x, the controller needs to wait t_{MRD} after the last control word access, before further access to the DRAM can take place. For any changes to the clock timing (RC02: bit DA3, and RC0A/RC3x) this settling may take up to tSTAB time. All chip select inputs, DCS[n:0]_n, must be kept HIGH during that time.

The DDR4RCD01 allocates decoding for up to 16 4-bit words of control bits (RC00 through RC0F) and up to 15 8-bit words of control bits. Selection of each word of 4-bit control bits is presented on inputs DA4 through DA12. Data to be written into the 4-bit configuration registers need to be presented on DA0 .. DA3. Selection of each word of 8-bit control bits is presented on inputs DA8 through DA12. Data to be written into the 8-bit configuration registers need to be presented on DA0 .. DA7. Bits DA[16:14] must be LOW and at least one DCKEn input must be HIGH for a valid access. If register CKE power down feature is disabled, DCKEn inputs are don't care (either HIGH or LOW), and are forwarded to the QxCKEn outputs. The DODT[1:0] inputs are also don't care (can be either HIGH or LOW), and are forwarded to the QxODT[1:0] outputs. Address and command parity is checked during control word write operations unless parity is disabled in the Parity Control Word. ALERT_n is asserted and the command is ignored if a parity error is detected.

See JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state."

wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.	The module controller of the SK hynix Products in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state. For example, the SK hynix products are configured to drive the Alert_n signal, in either a HIGH or LOW state, to the error edge connection via the open drain output while the memory module is in Clock-to-CA training mode, e.g., the second mode. The Alert_n signal constitutes information related to the Clock-to-CA training sequences.

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state."

2.12 CA Bus Training Modes

The DDR4RCD01 supports several training modes (selected in Table 35, "RC0C: Training Control Word") in order to assist the memory controller in aligning the incoming command/address and control signals optimally to the input clock signal CK_t/CK_t. These training modes are only available if a non-zero latency adder has been selected.

In Clock-to-CA training mode the DDR4RCD01 ORs all enabled Dn inputs[1] every other cycle together and loops back the result to the ALERT_n output pin. In this mode, the DPAR input is sampled at the same time as the other Dn inputs. The ALERT_n latency relative to the DQn inputs is the same 3 cycles as in the normal parity mode. During any of the CA bus training modes, QCA/QxCKEn and QxODTn hold their previous values and parity checking is disabled.

The memory controller can use the Clock-to-CA training mode and feedback from the DDR4RCD01 to adjust the CK_t-CK_c to Dn relationship analogous to the write leveling sequence which adjusts the DQS-DQS_n to CK_t-CK_c relationship. The memory controller writes consecutive sequences of all '1's and all '0's on the CA bus and pulls in the Dn timing until the DDR4RCD01 samples all Dn inputs as 0, which is indicated with the LOW assertion of ALERT_n. This position indicates the start position of a cumulative CA bus "eye opening". The memory controller advances the clock position or pulls in the Dn timing until the DDR4RCD01 samples at least one input as '1', which is indicated by ALERT_n remaining high three cycles after the last command. This position indicates the end position of a cumulative CA bus "eye opening". The memory controller can now position either the clock phase or the Dn input timing so that the clock edge is in the middle of this "eye opening" to achieve equal amounts of setup and hold time relative to the clock edge.

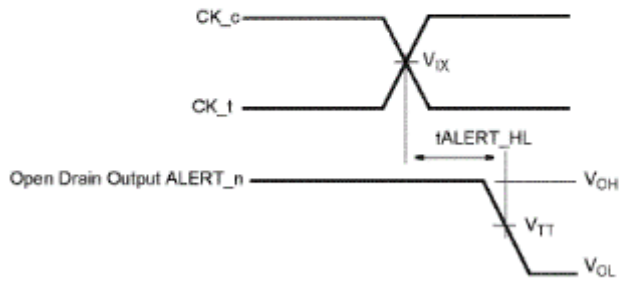
Figure 22 shows three sampling phase positions where the loopback ALERT_n pin transmits either a consistent 0 output, a randomly toggling 1/0 output or a consistent 1 output, indicating sampling positions at the LOW time, the transition time or the HIGH time of the inputs, respectively.

The memory controller can use the DCS0_n, DCS1_n, DCKE0, DCKE1, DODT0 and DODT0 loop back modes in similar fashion. In each of these modes a single input signal is looped back to the ALERT_n output and the memory controller can determine the optimal clock position for each of the control signals that are used for a particular DIMM. Once the optimal clock position for all CMD/ADDR and control inputs has been established, the memory controller can determine the best clock position for the whole set of input signals or potentially move the timing of individual control signals around to increase either setup or hold margins relative to the clock edge.

See JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state."

	Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows: • CA Signals = QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2, QxPAR • Control Signals = QxCKE0/1, QxODT0/1, QxC2, QxCS[1:0]_n for Dual CS mode, QxCS[3:0] • CK = Yn_t - Yn_c  **Figure 72 — Voltage waveforms, tALERT_HL Measurement** *See* JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state."

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	$V_{DD}/2$	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS[2] differential	Redriven clock
Reset output	QRST_n	CMOS[2]	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR QBPAR	CMOS[2]	Redriven parity[3]
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
	SDA	Open drain I/O	

See JEDEC RCD01 Specification (annotation added).

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state."

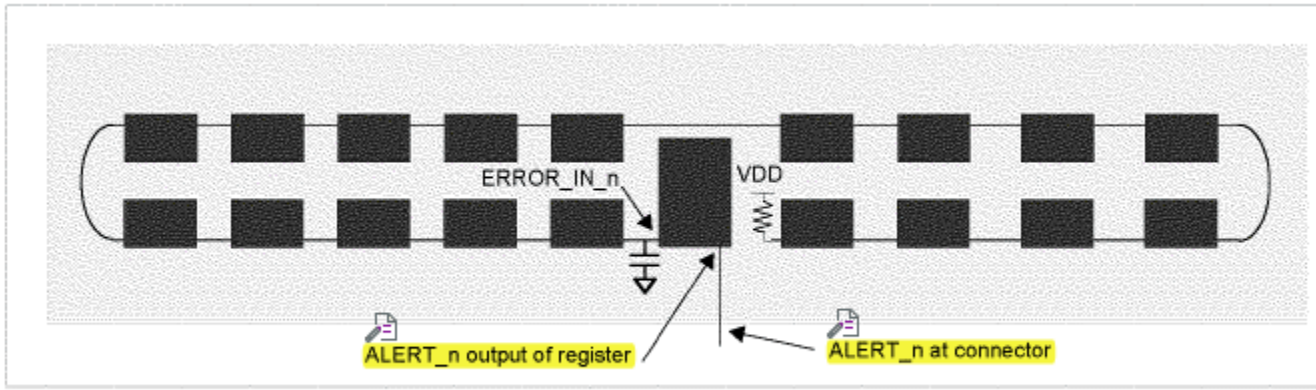


Figure 16 — Example Wiring of the ALERT_n Function

JEDEC RDIMM Standard (annotations added).

The Alert_n signal provides information related to the one or more training sequences. For example, while in Clock-to-CA training mode, the IDT 4RCD0124KC0 RCD ORs all enabled Dn inputs from the memory controller and then outputs the result of that OR operation to the memory controller via the Alert_n pin. The module controller of the SK hynix Products drives the open drain output and the error edge connection to one of two states.

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state."

2.12 CA Bus Training Modes

The DDR4RCD01 supports several training modes (selected in Table 35, "RC0C: Training Control Word") in order to assist the memory controller in aligning the incoming command/address and control signals optimally to the input clock signal CK_t/CK_t. These training modes are only available if a non-zero latency adder has been selected.

In Clock-to-CA training mode the DDR4RCD01 ORs all enabled Dn inputs[1] every other cycle together and loops back the result to the ALERT_n output pin. In this mode, the DPAR input is sampled at the same time as the other Dn inputs. The ALERT_n latency relative to the DQn inputs is the same 3 cycles as in the normal parity mode. During any of the CA bus training modes, QCA/QxCKEn and QxODTn hold their previous values and parity checking is disabled.

The memory controller can use the Clock-to-CA training mode and feedback from the DDR4RCD01 to adjust the CK_t-CK_c to Dn relationship analogous to the write leveling sequence which adjusts the DQS-DQS_n to CK_t-CK_c relationship. The memory controller writes consecutive sequences of all '1's and all '0's on the CA bus and pulls in the Dn timing until the DDR4RCD01 samples all Dn inputs as 0, which is indicated with the LOW assertion of ALERT_n. This position indicates the start position of a cumulative CA bus "eye opening". The memory controller advances the clock position or pulls in the Dn timing until the DDR4RCD01 samples at least one input as '1', which is indicated by ALERT_n remaining high three cycles after the last command. This position indicates the end position of a cumulative CA bus "eye opening". The memory controller can now position either the clock phase or the Dn input timing so that the clock edge is in the middle of this "eye opening" to achieve equal amounts of setup and hold time relative to the clock edge.

Figure 22 shows three sampling phase positions where the loopback ALERT_n pin transmits either a consistent 0 output, a randomly toggling 1/0 output or a consistent 1 output, indicating sampling positions at the LOW time, the transition time or the HIGH time of the inputs, respectively.

The memory controller can use the DCS0_n, DCS1_n, DCKE0, DCKE1, DODT0 and DODT0 loop back modes in similar fashion. In each of these modes a single input signal is looped back to the ALERT_n output and the memory controller can determine the optimal clock position for each of the control signals that are used for a particular DIMM. Once the optimal clock position for all CMD/ADDR and control inputs has been established, the memory controller can determine the best clock position for the whole set of input signals or potentially move the timing of individual control signals around to increase either setup or hold margins relative to the clock edge.

See JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 1

"wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state."

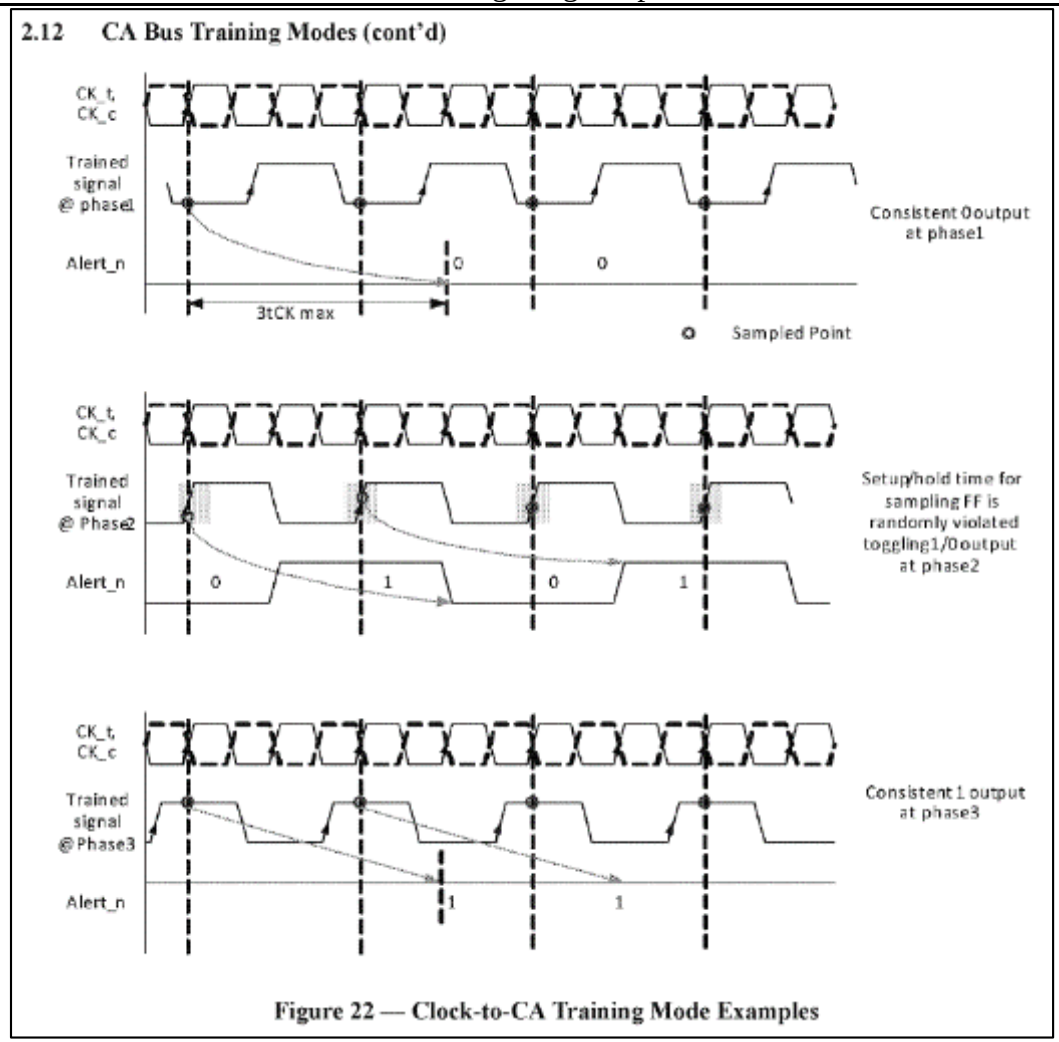
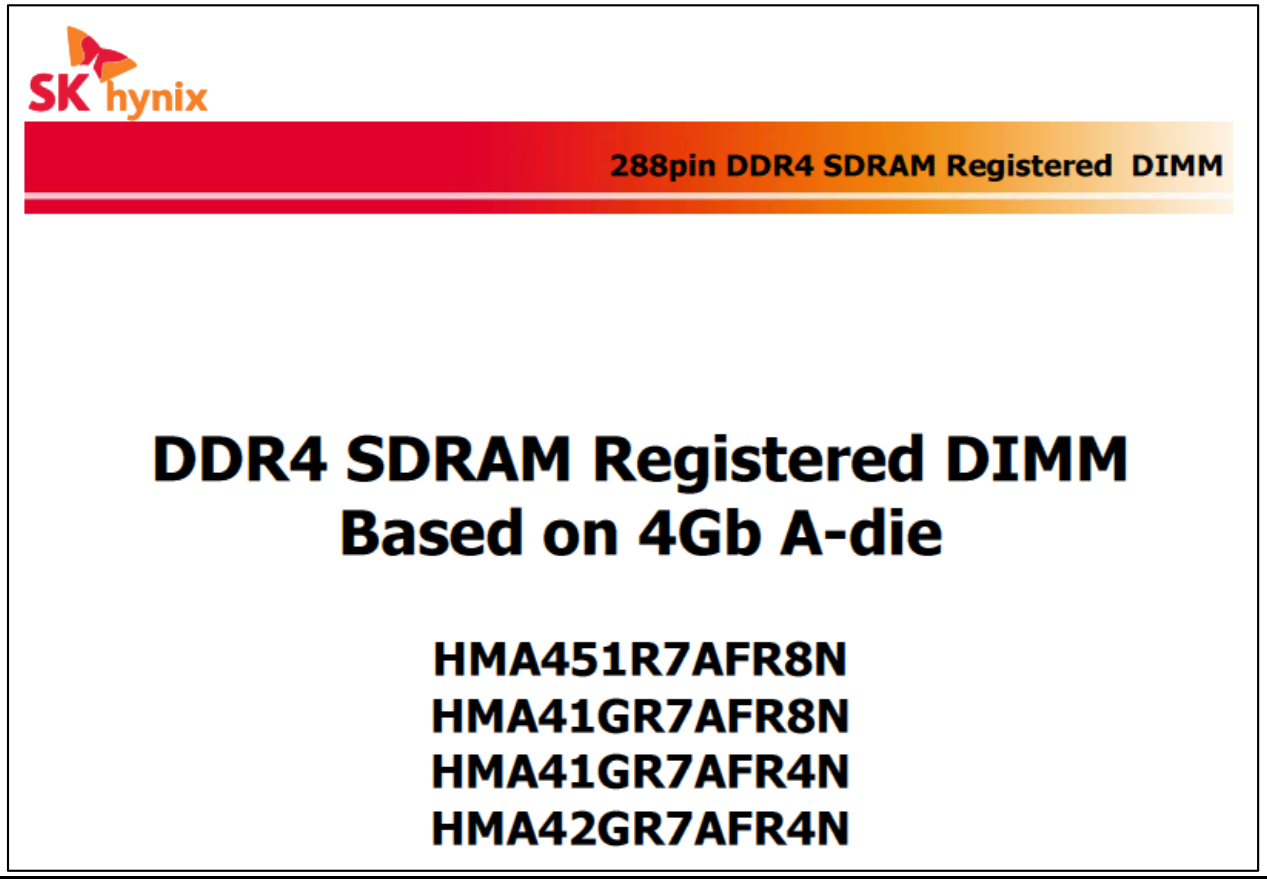


Figure 22 — Clock-to-CA Training Mode Examples

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 10

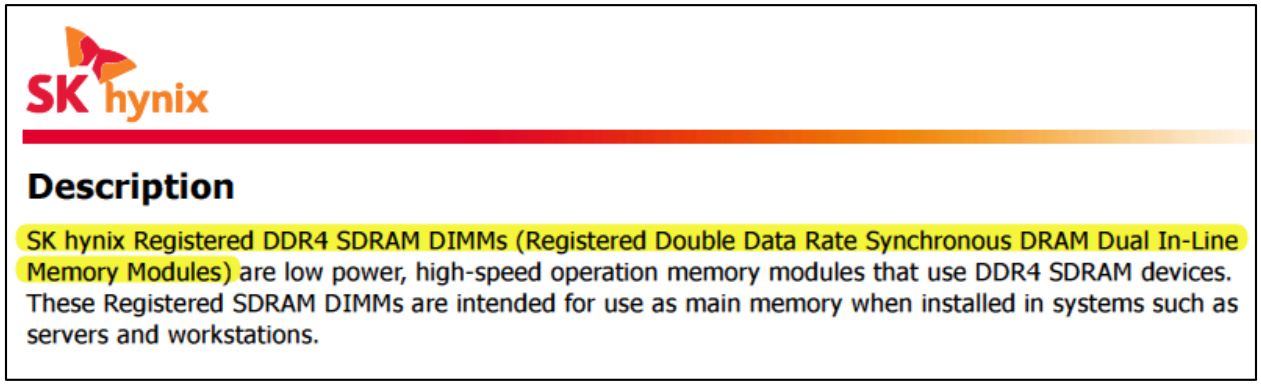
"10. A memory module operable with a memory controller of a host system, comprising:"

10. A memory module operable with a memory controller of a host system, comprising:	The SK hynix Products are memory modules operable with a memory controller of a host system. For example, the SK hynix Products are DDR4 registered dual in-line memory modules ("RDIMM"). (Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD). 

U.S. Patent No. 10,474,595: Claim 10

"10. A memory module operable with a memory controller of a host system, comprising:"

SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet, at 1.

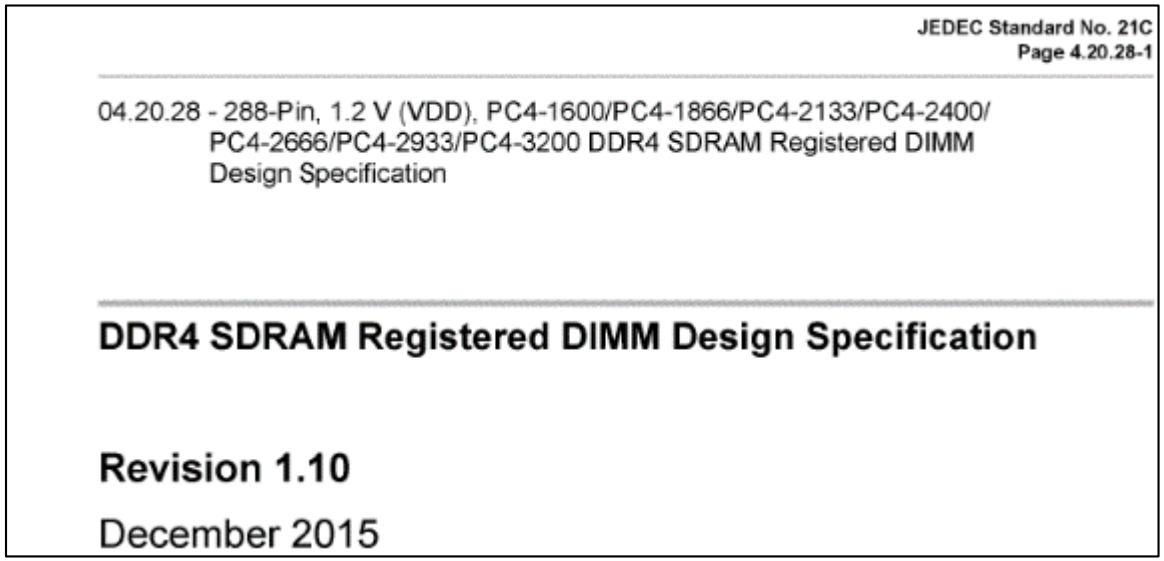


SK hynix

Description

SK hynix Registered DDR4 SDRAM DIMMs (Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Registered SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 3 (annotation added).



JEDEC Standard No. 21C
Page 4.20.28-1

04.20.28 - 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-2933/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification

DDR4 SDRAM Registered DIMM Design Specification

Revision 1.10

December 2015

JEDEC RDIMM Specification.

U.S. Patent No. 10,474,595: Claim 10

"10. A memory module operable with a memory controller of a host system, comprising:"

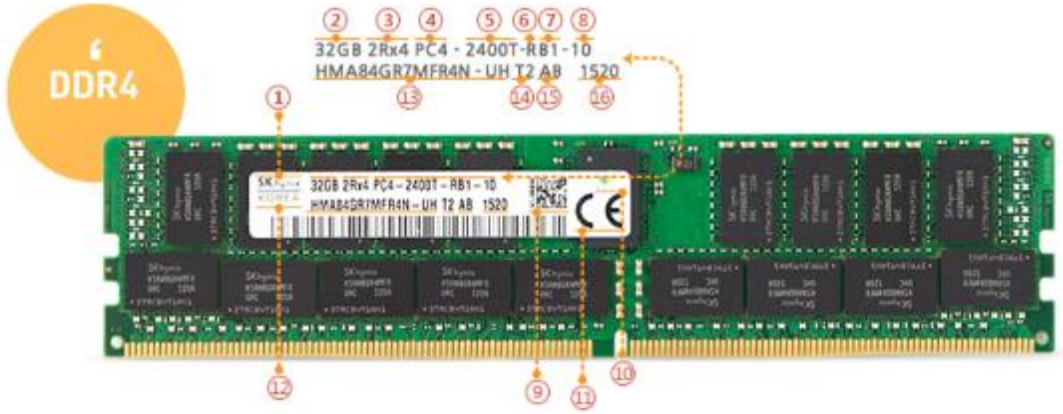
1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Registered, Double Data Rate, Synchronous SDRAM Dual In-Line Memory Modules (DDR4 SDRAM RDIMMs). These DDR4 Registered DIMMs (RDIMMs) are intended for use as main memory when installed in PCs.

JEDEC RDIMM Specification (annotation added).

The SK hynix HMA42GR7AFR4N-UHTD is manufactured according to JEDEC specifications:

Label Info. DDR4



See SKH DDR4 Module Label Info at 3.

(6)	Module Type	U : 288pin Unbuffered DIMM R : 288pin Registered DIMM S : 260 pin Unbuffered SO-DIMM L : 288pin LRDIMM N : 288pin NVDIMM
(7)	Gerber Revision	JEDEC Reference design file used for this design
(8)	SPD Revision	JEDEC SPD Revision Encoding and Additions level

See SKH DDR4 Module Label Info at 3.

U.S. Patent No. 10,474,595: Claim 10

"10. A memory module operable with a memory controller of a host system, comprising:"

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

The SK hynix Products are intended for use as main memory in systems such as servers and workstations.

JEDEC Standard No. 21C
Page 4.20.28-5

1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Registered, Double Data Rate, Synchronous SDRAM Dual In-Line Memory Modules (DDR4 SDRAM RDIMMs). These DDR4 Registered DIMMs (RDIMMs) are intended for use as main memory when installed in PCs.

JEDEC RDIMM Standard (annotation added).

SK hynix

Description

SK hynix Registered DDR4 SDRAM DIMMs (Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Registered SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 3 (annotations added).

The SK hynix Products are operable with a memory controller of a host system. For example, the SK hynix Products include a printed circuit board (PCB) for communicating signals between (e.g., to/from) the memory module and the memory controller of a host system.

U.S. Patent No. 10,474,595: Claim 10

"10. A memory module operable with a memory controller of a host system, comprising:"

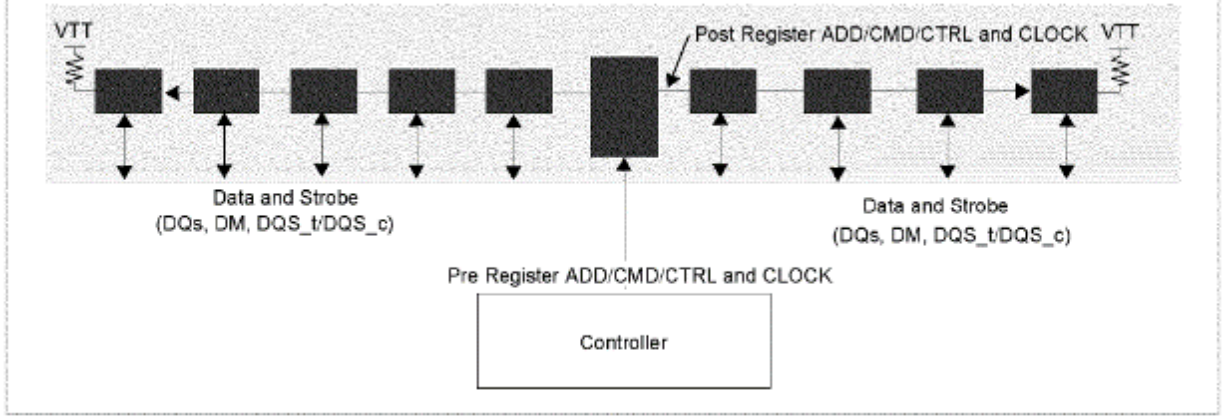


Figure 4 — Example RDIMM Topologies

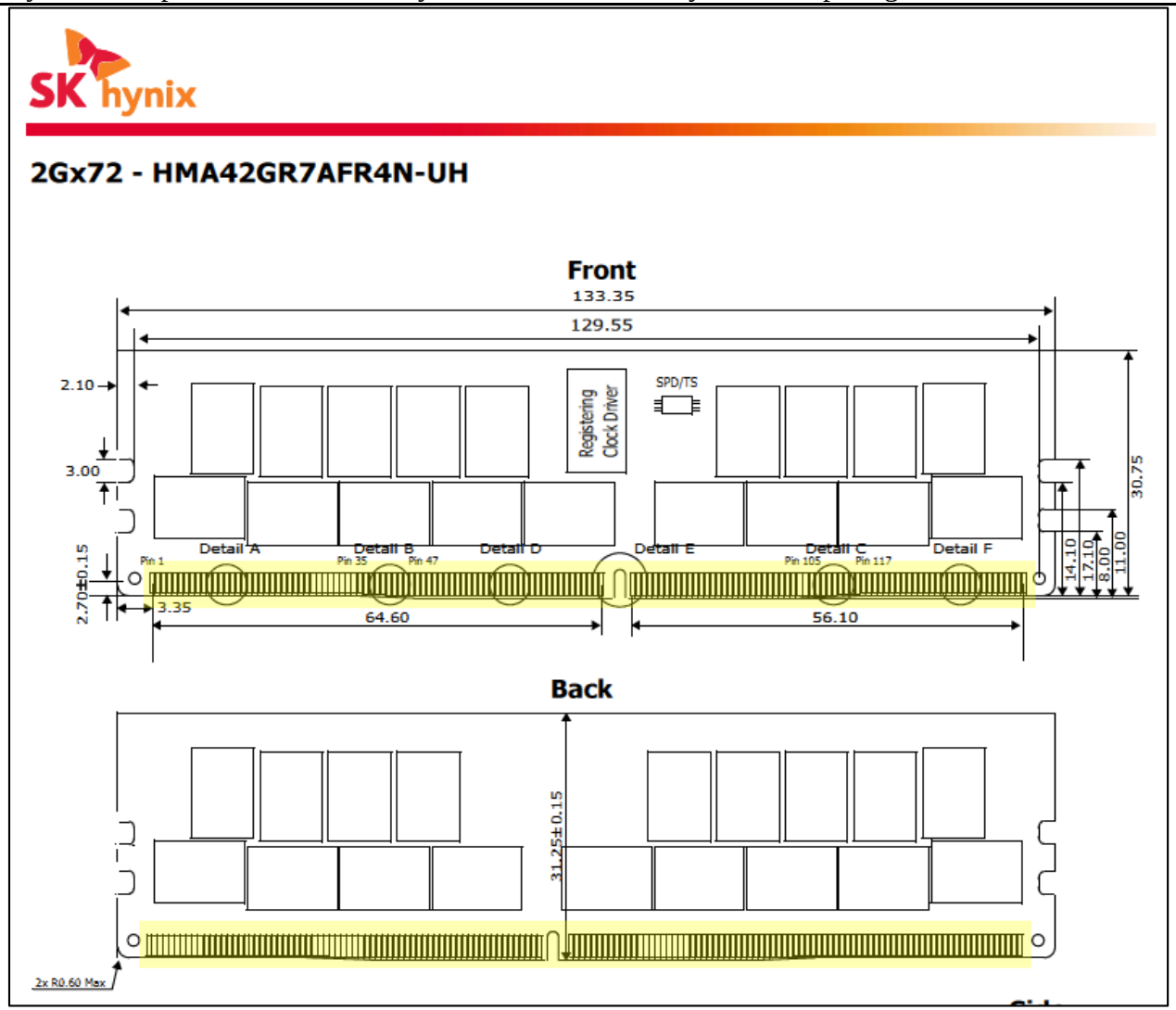
JEDEC RDIMM Specification.

For example, the SK hynix Products contain contacts for connecting to a memory controller of a computer system.

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

U.S. Patent No. 10,474,595: Claim 10

"10. A memory module operable with a memory controller of a host system, comprising:"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 81 (annotations added).

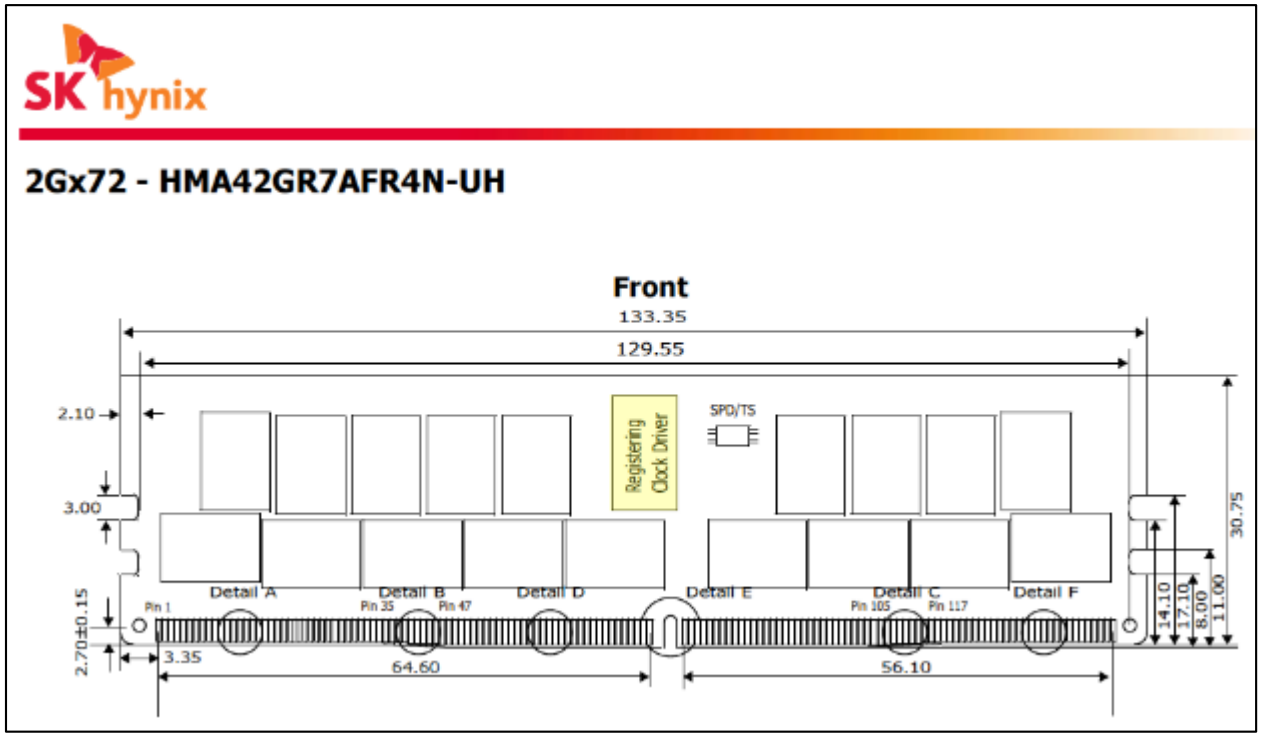
For example, the SK hynix include a JEDEC RCD01 compliant register clock driver ("RCD") that is operable with a memory controller of a host system.

> Some modules have lower current requirements. Any specific module must meet the SDRAM and DDR4RCD01 voltage requirements for its worst case supply currents.

U.S. Patent No. 10,474,595: Claim 10

"10. A memory module operable with a memory controller of a host system, comprising:"

See, e.g., JEDEC RDIMM Standard (annotation added).



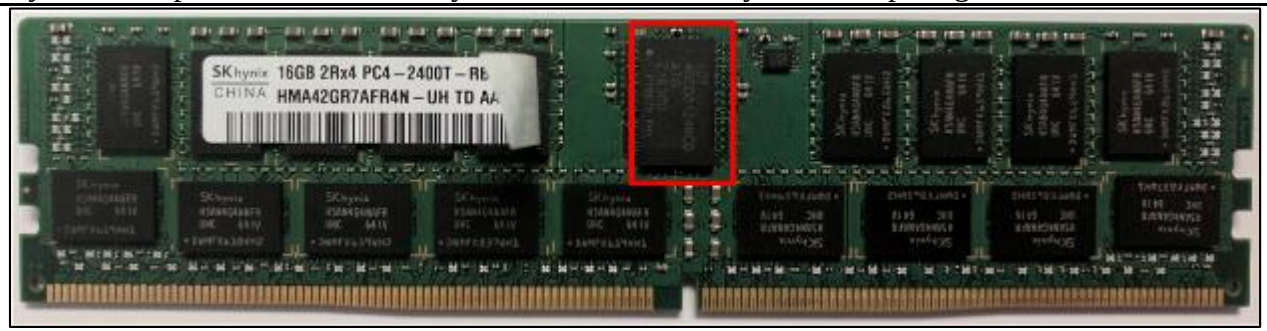
SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 81 (annotations added).

Specifically, the SK hynix Products contain a IDT 4RCD0124KC0 RCD.

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

U.S. Patent No. 10,474,595: Claim 10

"10. A memory module operable with a memory controller of a host system, comprising:"

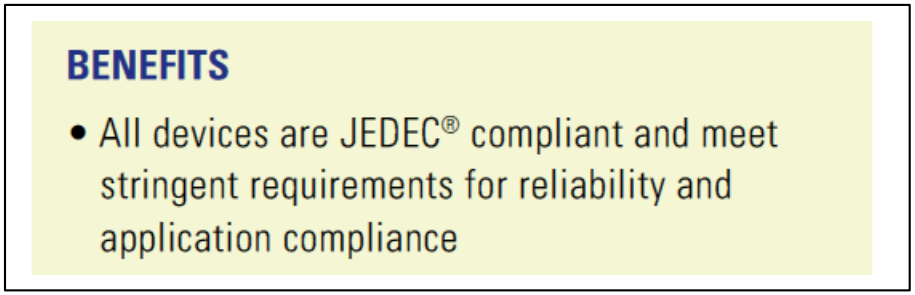


(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

The IDT 4RCD0124KC0 RCD is JEDEC Compliant.

See 4RCD0124K DDR4 Register Clock Driver Webpage at 1.

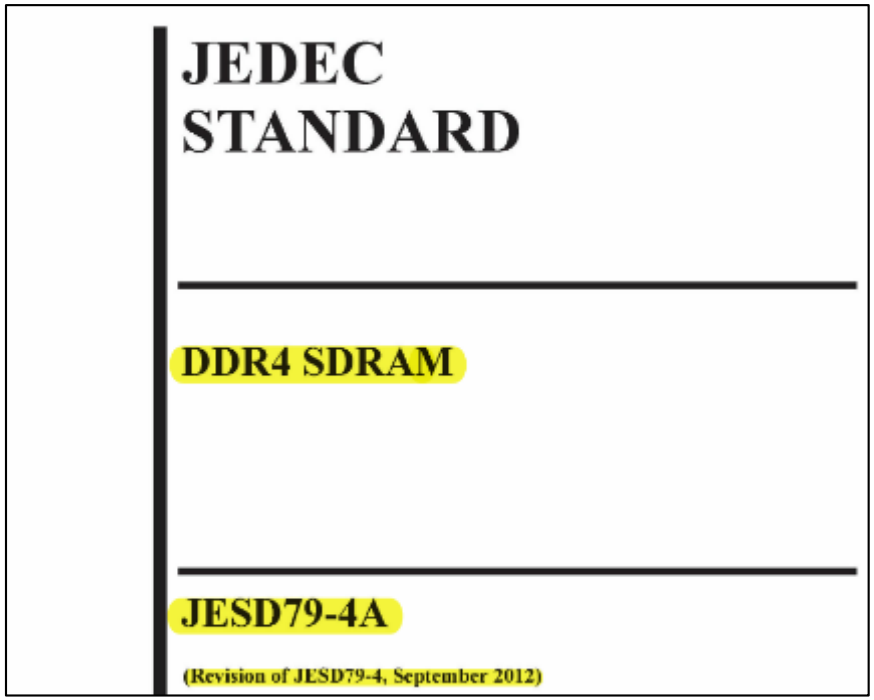


IDT Leader in Server Memory Chipsets at 1.

U.S. Patent No. 10,474,595: Claim 10

"10. A memory module operable with a memory controller of a host system, comprising:"

The SK hynix Products further comply with the JEDEC SDRAM Standard, JESD79-4.



JEDEC DDR4 SDRAM Specification (annotations added).
See also SKH DDR4 Device Operation at 1.

The RCD is operatively coupled to the memory controller of the host system.

U.S. Patent No. 10,474,595: Claim 10

"10. A memory module operable with a memory controller of a host system, comprising:"

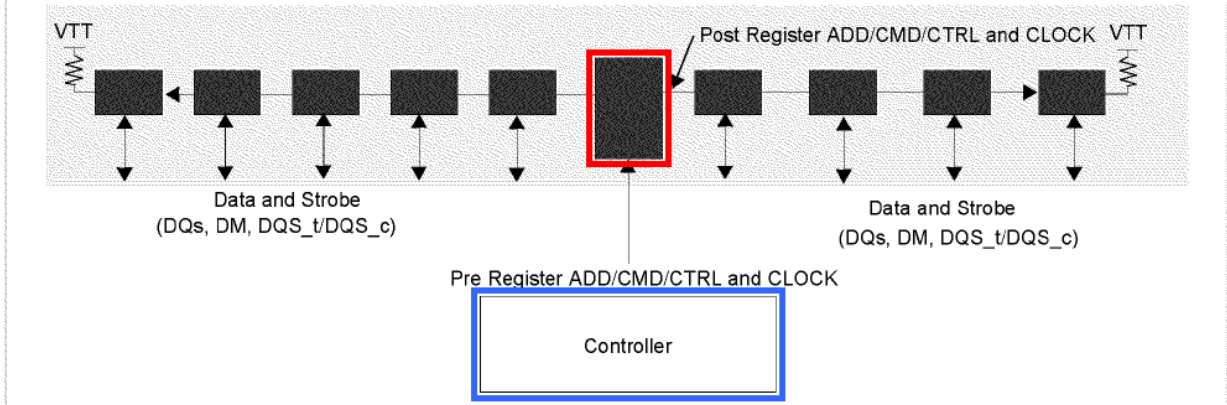


Figure 4 — Example RDIMM Topologies

JEDEC RDIMM Standard (annotation added).

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;	The SK hynix Products include a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections. The SK hynix Products include a printed circuit board (PCB) having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller. For example, the PCB of the SK hynix Products is configured to fit into a corresponding slot of the host system. SK hynix **Description** SK hynix Registered DDR4 SDRAM DIMMs (Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Registered SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations. SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 3 (annotation added). JEDEC Standard No. 21C Page 4.20.28-5 **1 Product Description** This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Registered, Double Data Rate, Synchronous SDRAM Dual In-Line Memory Modules (DDR4 SDRAM RDIMMs). These DDR4 Registered DIMMs (RDIMMs) are intended for use as main memory when installed in PCs. JEDEC RDIMM Standard (annotation added).

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

For example, as illustrated in the figures below, the SK hynix Products include a printed circuit board (PCB) having edge connections for communicating signals between (e.g., to/from) the memory module and the memory controller of the host system, e.g., electrical communication between the memory module and the memory controller.

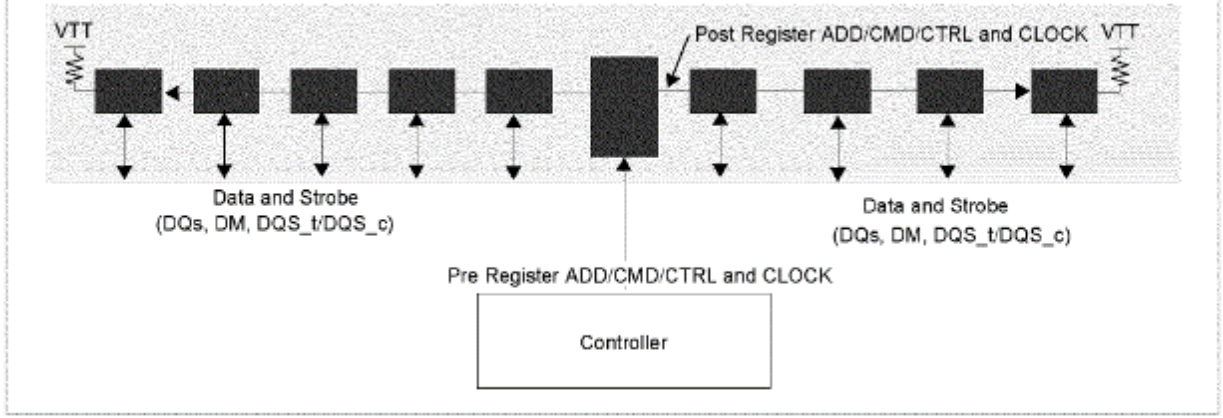


Figure 4 — Example RDIMM Topologies

JEDEC RDIMM Standard.

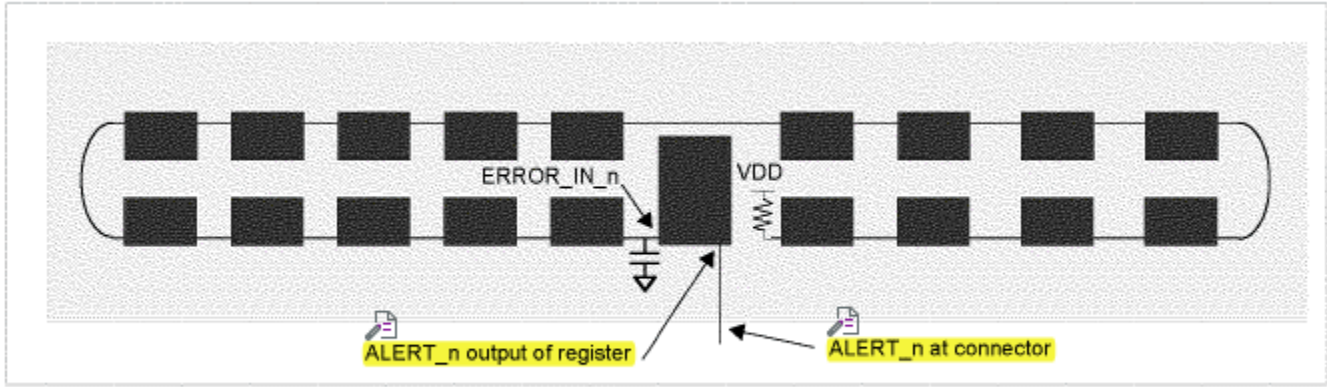


Figure 16 — Example Wiring of the ALERT_n Function

JEDEC RDIMM Standard (annotations added).

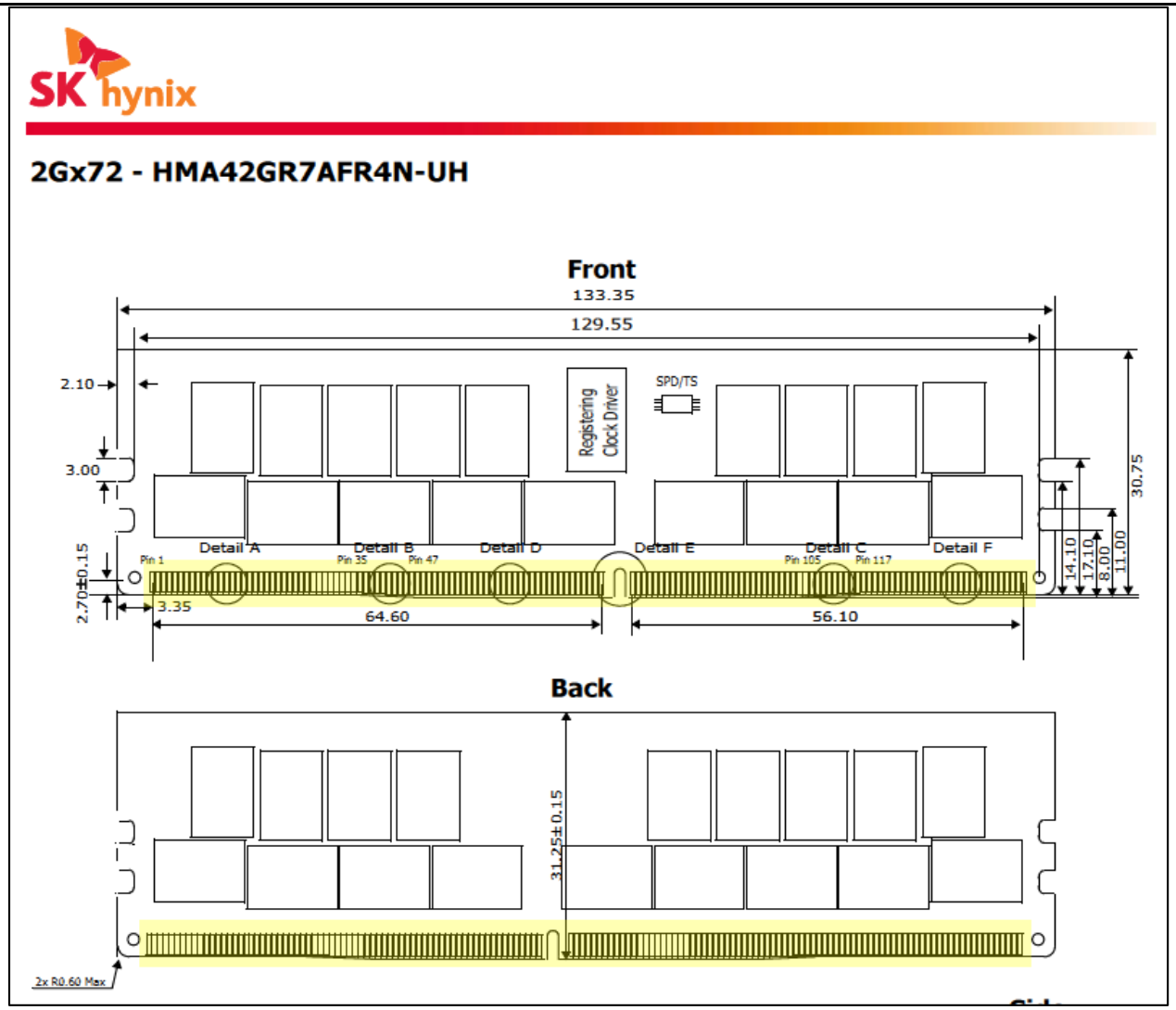
U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

	For example, the SK hynix Products contain contacts (e.g., edge connections) for connecting to a memory controller of a computer system. (Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 81 (annotations added).

The edge connections of the SK hynix Products include a first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections.

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

JEDEC Standard No. 21C
Page 4.20.28-10

Table 5 — DDR4 288 Pin RDIMM Pin Wiring Assignments

Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
12 V, NC	1	145	12 V, NC	CK0_t	74	218	CK1_t
VSS	2	146	VREFCA	CK0_c	75	219	CK1_c
DQ4	3	147	VSS	VDD	76	220	VDD
VSS	4	148	DQ5	VTT	77	221	VTT
DQ0	5	149	VSS		KEY		
VSS	6	150	DQ1				
TDQS9_t, DQS9_t, DM0_n, DBI0_n, NC	7	151	VSS	EVENT_n	78	222	PARITY
TDQS9_c, DQS9_c, NC	8	152	DQS0_c	A0	79	223	VDD
VSS	9	153	DQS0_t	VDD	80	224	BA1
DQ6	10	154	VSS	BA0	81	225	A10/AP
VSS	11	155	DQ7	RAS_n/A16	82	226	VDD
DQ2	12	156	VSS	VDD	83	227	RFU
VSS	13	157	DQ3	CS0_n	84	228	WE_n/A14
DQ12	14	158	VSS	VDD	85	229	VDD

JEDEC RDIMM Standard (showing, for example, WE_n, A0, DQ4).

ACT_n	62	206	VDD	TDQS16_c, DQS16_c, NC	133	277	DQS7_c
BG0	63	207	BG1	VSS	134	278	DQS7_t
VDD	64	208	ALERT_n	DQ62	135	279	VSS
A12/BC_n	65	209	VDD	VSS	136	280	DQ63
A9	66	210	A11	DQ58	137	281	VSS
VDD	67	211	A7	VSS	138	282	DQ59
A8	68	212	VDD	SA0	139	283	VSS
A6	69	213	A5	SA1	140	284	VDDSPD
VDD	70	214	A4	SCL	141	285	SDA
A3	71	215	VDD	VPP	142	286	VPP
A1	72	216	A2	VPP	143	287	VPP
VDD	73	217	VDD	RFU	144	288	VPP

JEDEC RDIMM Standard (showing, for example, ALERT_n).

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

SK hynix

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
37	VSS	181	DQ29	108	DQ40	252	VSS
38	DQ24	182	VSS	109	VSS	253	DQ41
39	VSS	183	DQ25	110	TDQS14_t, DQS14_t, DM5_n, DBI5_n	254	VSS
40	TDQS12_t, DQS12_t, DM3_n, DBI3_n	184	VSS	111	TDQS14_c, DQS14_c	255	DQS5_c
41	TDQS12_c, DQS12_c	185	DQS3_c	112	VSS	256	DQS5_t
42	VSS	186	DQS3_t	113	DQ46	257	VSS
43	DQ30	187	VSS	114	VSS	258	DQ47
44	VSS	188	DQ31	115	DQ42	259	VSS
45	DQ26	189	VSS	116	VSS	260	DQ43
46	VSS	190	DQ27	117	DQ52	261	VSS
47	CB4	191	VSS	118	VSS	262	DQ53
48	VSS	192	CB5	119	DQ48	263	VSS
49	CB0	193	VSS	120	VSS	264	DQ49
50	VSS	194	CB1	121	TDQS15_t, DQS15_t, DM6_n, DBI6_n	265	VSS
51	TDQS17_t, DQS17_t, DM8_n, DBI8_n	195	VSS	122	TDQS15_c, DQS15_c	266	DQS6_c
52	TDQS17_c, DQS17_c	196	DQS8_c	123	VSS	267	DQS6_t
53	VSS	197	DQS8_t	124	DQ54	268	VSS
54	CB6	198	VSS	125	VSS	269	DQ55
55	VSS	199	CB7	126	DQ50	270	VSS
56	CB2	200	VSS	127	VSS	271	DQ51
57	VSS	201	CB3	128	DQ60	272	VSS
58	RESET_n	202	VSS	129	VSS	273	DQ61
59	VDD	203	CKE1, NC	130	DQ56	274	VSS
60	CKE0	204	VDD	131	VSS	275	DQ57
61	VDD	205	RFU	132	TDQS16_t, DQS16_t, DM7_n, DBI7_n	276	VSS
62	ACT_n	206	VDD	133	TDQS16_t, DQS16_c	277	DQS7_c
63	BG0	207	BG1	134	VSS	278	DQS7_t
64	VDD	208	ALERT_n	135	DQ62	279	VSS
65	A12/BC_n	209	VDD	136	VSS	280	DQ63
66	A9	210	A11	137	DQ58	281	VSS
67	VDD	211	A7	138	VSS	282	DQ59
68	A8	212	VDD	139	SA0	283	VSS
69	A6	213	A5	140	SA1	284	VDDSPD
70	VDD	214	A4	141	SCL	285	SDA
71	A3	215	VDD	142	VPP	286	VPP
72	A1	216	A2	143	VPP	287	VPP
73	VDD	217	VDD	144	RFU	288	VPP

SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 10 (showing separate pin connections for data, address, control, and ALERT_n).

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

For example, the SK hynix Products include first edge connections for communicating data signals between the memory module and the memory controller of the host system. For example, the SK hynix Products include the following input/output pins:

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I^2C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I^2C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I^2C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS9_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	DM0_n-DM8_n	Data Mask
DQS0_c–DQS17_c	Data Buffer data strobes	RESET_n	Set Register and SDRAMs to a Known State

DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

DQS0_t-DQS17_t, DQS0_c-DQS17_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

JEDEC RDIMM Standard.
See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 5, 7.

The DQ and DQS signals are used to communicate data signals between the memory module and the memory controller of the host system.

JEDEC Standard No. 21C
Page 4.20.28-19

6 DIMM Design Details

6.1 Signal Groups

This specification categorizes DDR4 SDRAM signals into six groups. Figure 4 illustrates the DIMM wiring. All signal groups, except DQ, implement a fly-by topology.

The signal groups are:

1. DQ and DQS signals connector to SDRAM

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

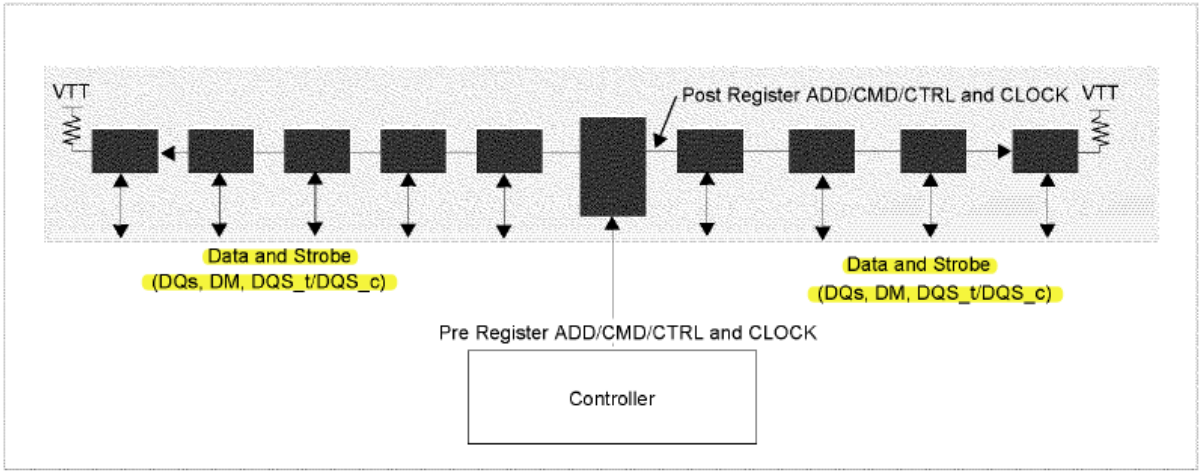


Figure 4 — Example RDIMM Topologies

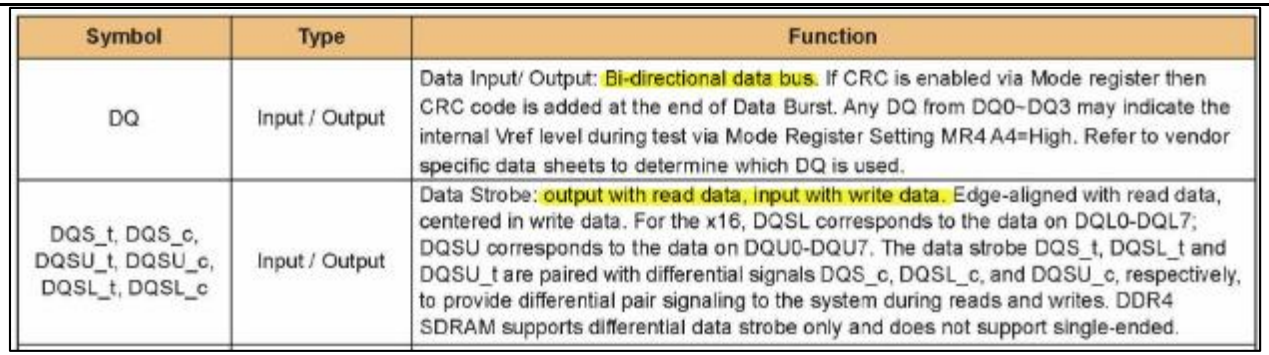
JEDEC RDIMM Standard (annotations added).

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

JEDEC DDR4 SDRAM Specification (annotations added).
See also SKH DDR4 Device Operation at 7.

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

	 JEDEC DDR4 SDRAM Specification (annotations added). *See also* SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 7.

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

JEDEC Standard No. 79-4A
Page 86

4.24.1.2 READ Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 67 and is applied when the DLL is enabled and locked.

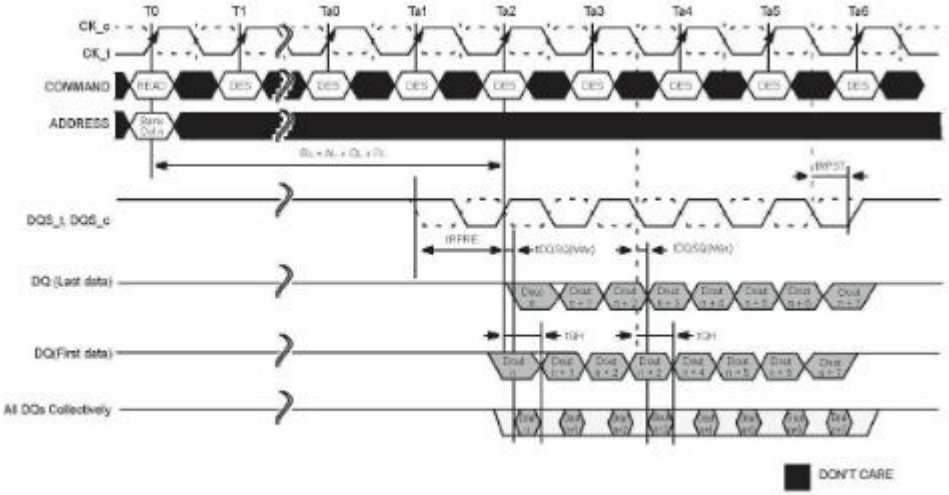
Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

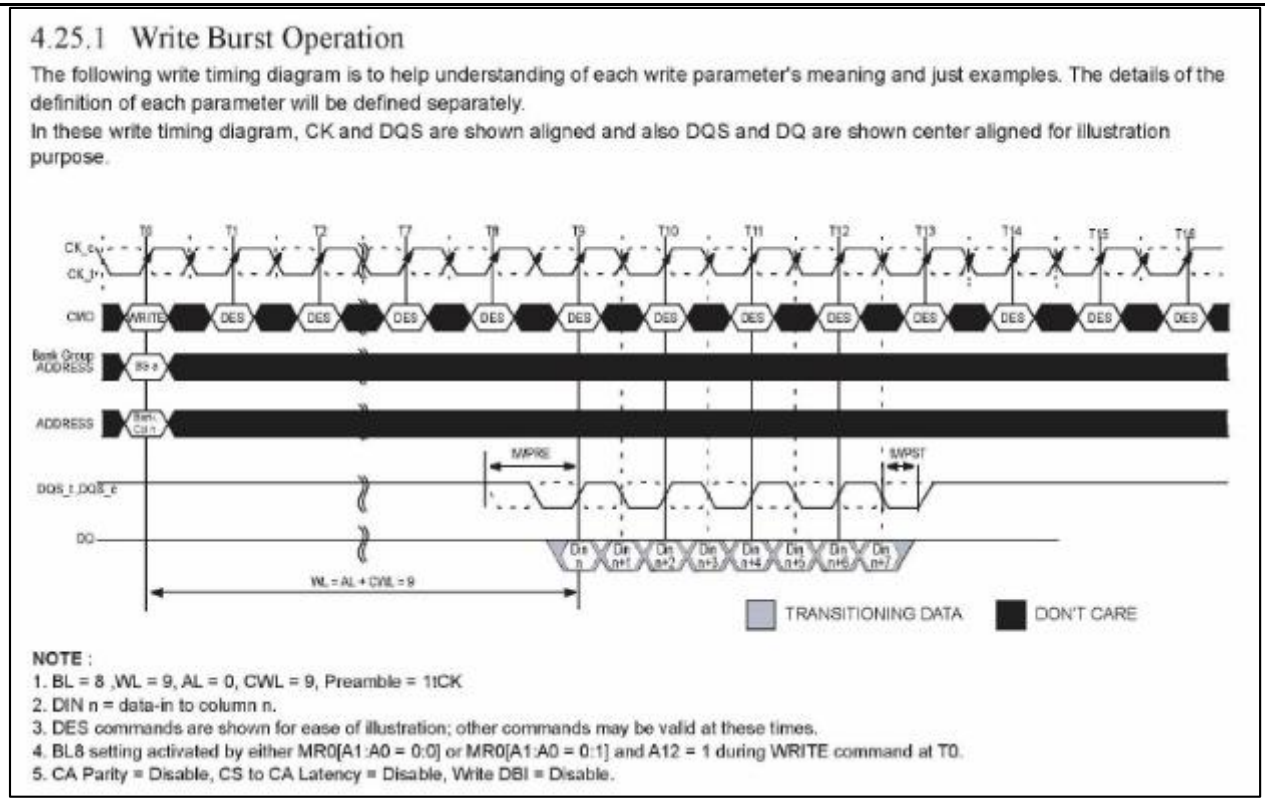
tDQSQ: both rising/falling edges of DQS, no tAC defined.



See, e.g., JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 97.

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"



4.25.1 Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.

In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.

NOTE :
1. BL = 8 ,WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

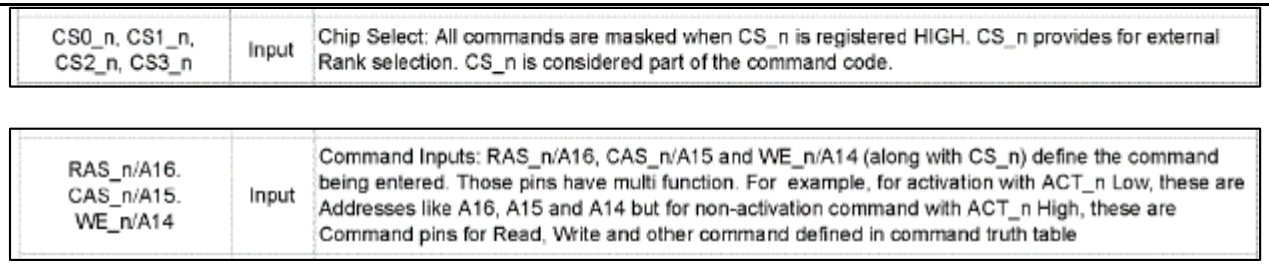
See, e.g., JEDEC DDR4 SDRAM Specification.
See also JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 126, 94-144.

The SK hynix Products also include second edge connections for communicating address and control signals from the memory controller of the host system. For example, the SK hynix Products include the following input pins:

A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.

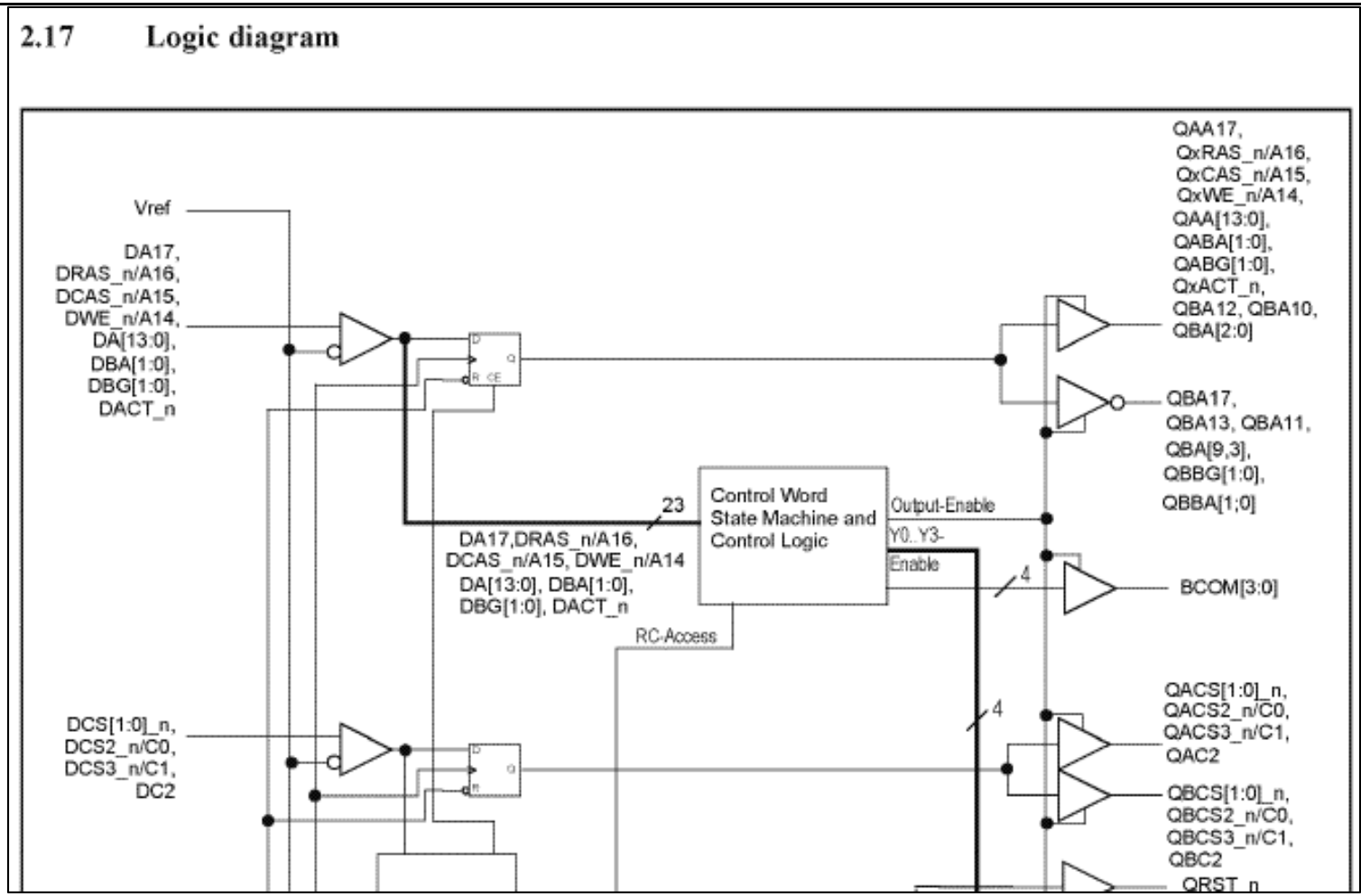
U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

	 JEDEC RDIMM Standard. *See also* SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 6.

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"



See JEDEC RCD01 Specification.

The PCB further includes an error edge connection in addition to the first set of edge connections and the second set of edge connections. For example, the SK hynix Products include the ALERT_n pin.

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

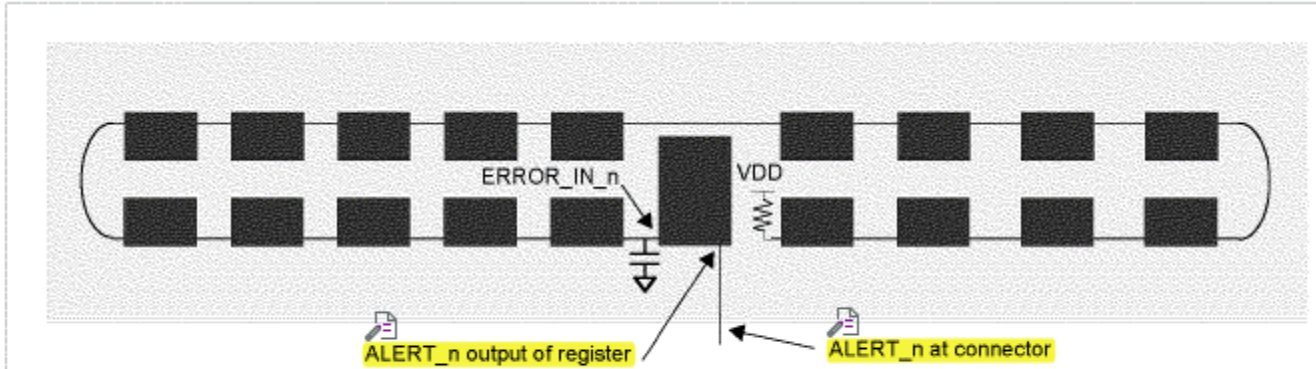


Figure 16 — Example Wiring of the ALERT_n Function

JEDEC RDIMM Standard (annotations added).

U.S. Patent No. 10,474,595: Claim 10

"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I²C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I²C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I²C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS9_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	DM0_n-DM8_n	Data Mask
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred.
CK0_t, CK1_t	Register clock input (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clocks input (negative line of differential pair)	RFU	Reserved for future use

JEDEC RDIMM Standard (annotations added).

ALERT_n	Output (Input)	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system.

JEDEC RDIMM Standard.

U.S. Patent No. 10,474,595: Claim 10

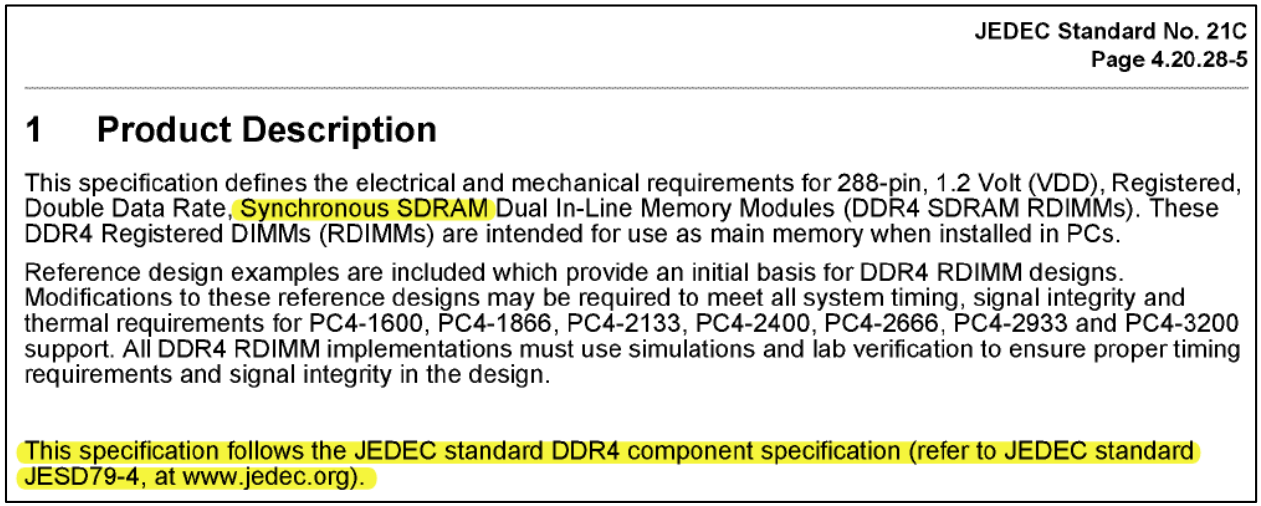
"a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;"

Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
TDQS12_t, DQS12_t, DM3_n, DBI3_n, NC	40	184	VSS	TDQS14_c, DQS14_c, NC	111	255	DQS5_c
TDQS12_c, DQS12_c, NC	41	185	DQS3_c	VSS	112	256	DQS5_t
VSS	42	186	DQS3_t	DQ46	113	257	VSS
DQ30	43	187	VSS	VSS	114	258	DQ47
VSS	44	188	DQ31	DQ42	115	259	VSS
DQ26	45	189	VSS	VSS	116	260	DQ43
VSS	46	190	DQ27	DQ52	117	261	VSS
CB4, NC	47	191	VSS	VSS	118	262	DQ53
VSS	48	192	CB5, NC	DQ48	119	263	VSS
CB0, NC	49	193	VSS	VSS	120	264	DQ49
VSS	50	194	CB1, NC	TDQS15_t, DQS15_t, DM6_n, DBI6_n, NC	121	265	VSS
TDQS17_t, DQS17_t, DM8_n, DBI8_n, NC	51	195	VSS	TDQS15_c, DQS15_c, NC	122	266	DQS6_c
TDQS17_c, DQS17_c, NC	52	196	DQS8_c	VSS	123	267	DQS6_t
VSS	53	197	DQS8_t	DQ54	124	268	VSS
CB6, NC	54	198	VSS	VSS	125	269	DQ55
VSS	55	199	CB7, NC	DQ50	126	270	VSS
CB2, NC	56	200	VSS	VSS	127	271	DQ51
VSS	57	201	CB3, NC	DQ60	128	272	VSS
RESET_n	58	202	VSS	VSS	129	273	DQ61
VDD	59	203	CKE1, NC	DQ56	130	274	VSS
CKE0	60	204	VDD	VSS	131	275	DQ57
VDD	61	205	RFU	TDQS16_t, DQS16_t, DM7_n, DBI7_n, NC	132	276	VSS
ACT_n	62	206	VDD	TDQS16_c, DQS16_c, NC	133	277	DQS7_c
BG0	63	207	BG1	VSS	134	278	DQS7_t
VDD	64	208	ALERT_n	DQ62	135	279	VSS
A12/BC_n	65	209	VDD	VSS	136	280	DQ63
A9	66	210	A11	DQ58	137	281	VSS
VDD	67	211	A7	VSS	138	282	DQ59
A8	68	212	VDD	SA0	139	283	VSS
A6	69	213	A5	SA1	140	284	VDDSPD
VDD	70	214	A4	SCL	141	285	SDA
A3	71	215	VDD	VPP	142	286	VPP
A1	72	216	A2	VPP	143	287	VPP
VDD	73	217	VDD	RFU	144	288	VPP

JEDEC RDIMM Standard (annotations added) (showing Alert_n at pin 208, separate and distinct from control, address, and data pins / edge connections).

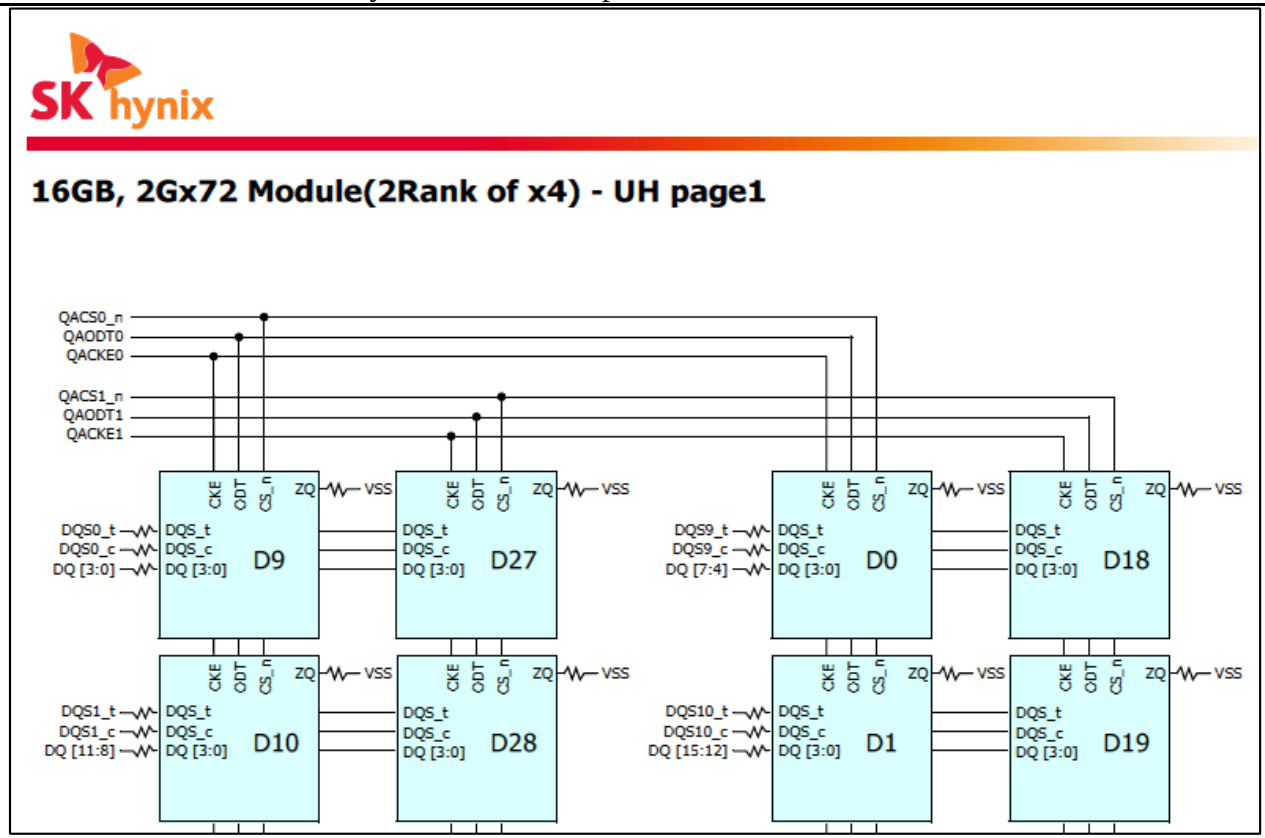
U.S. Patent No. 10,474,595: Claim 10

"dynamic random access memory elements on the printed circuit board;"

dynamic random access memory elements on the printed circuit board;	The SK hynix Products include dynamic random access memory elements on the printed circuit board. For example, the SK hynix Product includes a plurality of JEDEC-compliant synchronous dynamic random access memories ("SDRAMs").  JEDEC Standard No. 21C Page 4.20.28-5 1 Product Description This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Registered, Double Data Rate, Synchronous SDRAM Dual In-Line Memory Modules (DDR4 SDRAM RDIMMs). These DDR4 Registered DIMMs (RDIMMs) are intended for use as main memory when installed in PCs. Reference design examples are included which provide an initial basis for DDR4 RDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC4-1600, PC4-1866, PC4-2133, PC4-2400, PC4-2666, PC4-2933 and PC4-3200 support. All DDR4 RDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design. This specification follows the JEDEC standard DDR4 component specification (refer to JEDEC standard JESD79-4, at www.jedec.org). JEDEC RDIMM Standard (annotations added).

U.S. Patent No. 10,474,595: Claim 10

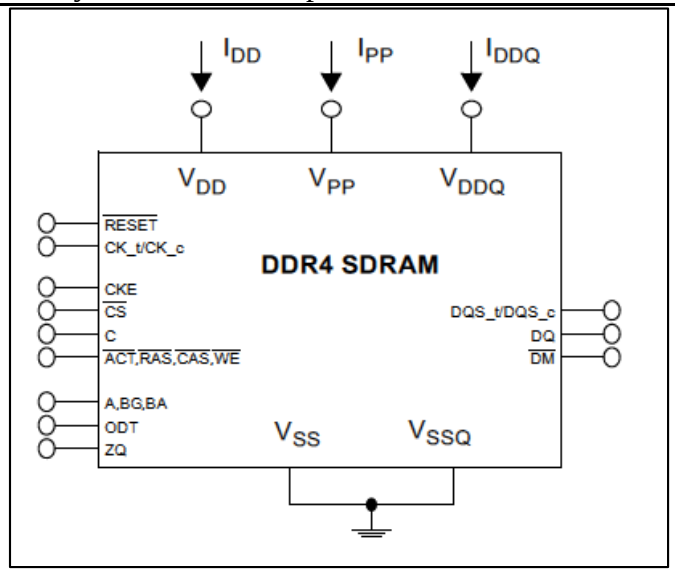
"dynamic random access memory elements on the printed circuit board;"



See SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 20 (showing SDRAM device D9, D27, D0, D18, D10, D28, D1, and D19).

U.S. Patent No. 10,474,595: Claim 10

"dynamic random access memory elements on the printed circuit board;"



See SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 55.

Specifically, the SK hynix HMA42GR7AFR4N-UHTD comprises 36 SDRAM components.

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD) (front side).

U.S. Patent No. 10,474,595: Claim 10

"dynamic random access memory elements on the printed circuit board;"

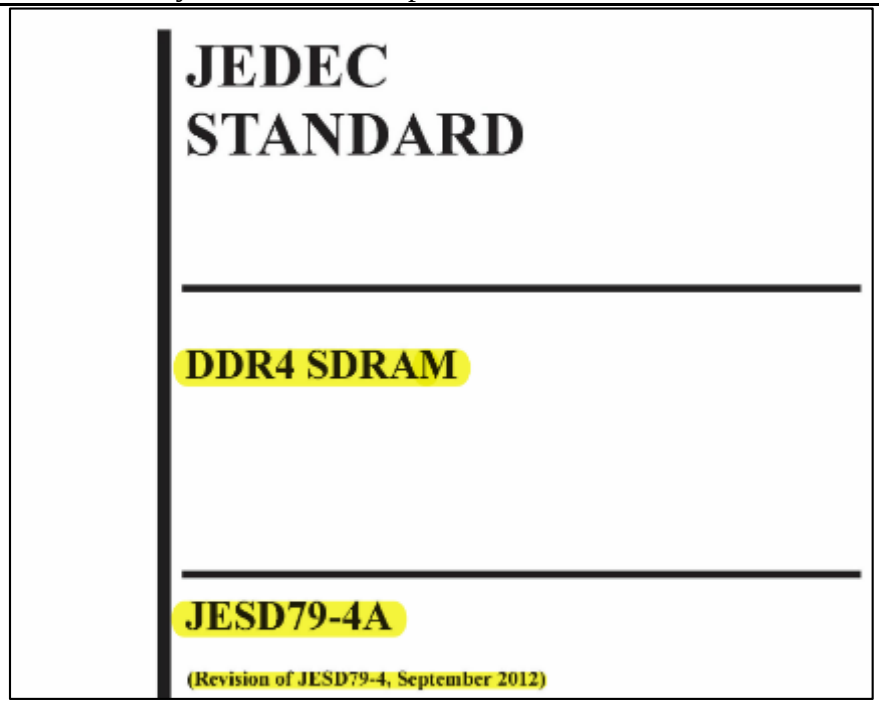
(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD) (back side).

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD) (SDRAM).

The SDRAM devices are JEDEC complaint.

U.S. Patent No. 10,474,595: Claim 10

"dynamic random access memory elements on the printed circuit board;"



JEDEC DDR4 SDRAM Specification (annotations added).
See also SKH DDR4 Device Operation at 1.

The SDRAM devices are outlined in red in the figure below.

U.S. Patent No. 10,474,595: Claim 10

"dynamic random access memory elements on the printed circuit board;"

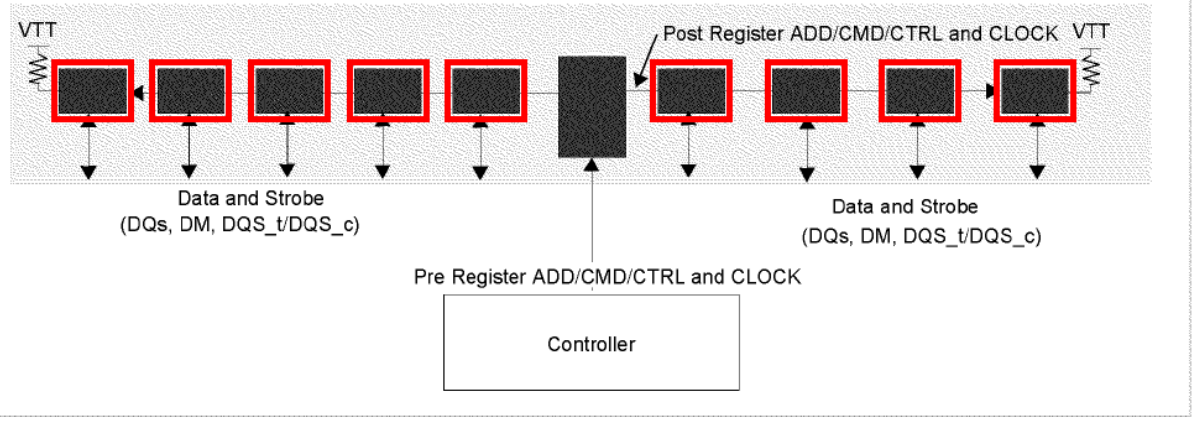
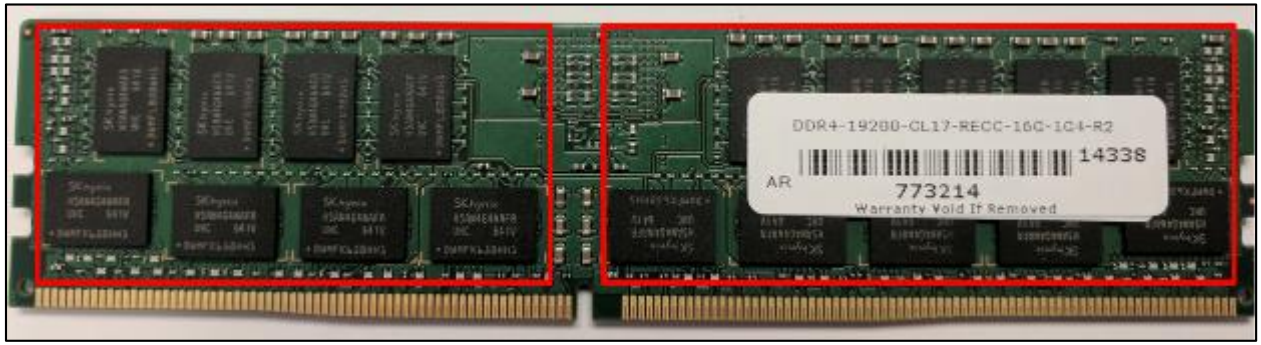


Figure 4 — Example RDIMM Topologies

JEDEC RDIMM Standard (annotations added).

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 65.

(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD) (front side).

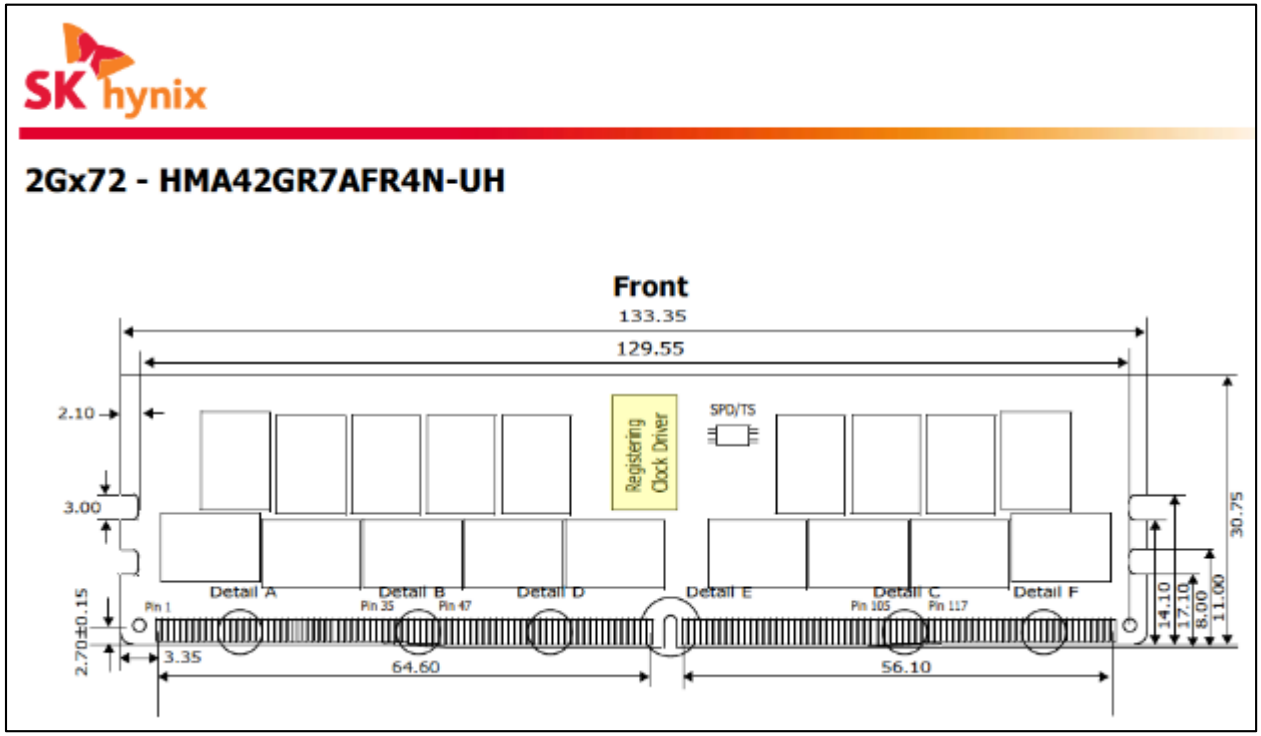


"dynamic random access memory elements on the printed circuit board;"

	(Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD) (back side).

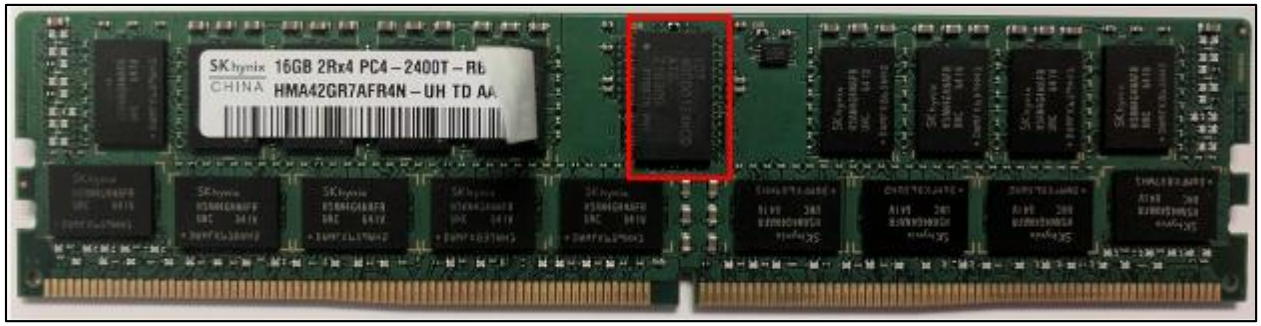
U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and	The SK hynix Products include a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection. The module controller of the SK hynix Products is configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state The SK hynix Products comprise a module controller on the printed circuit board. For example, the SK hynix Products contain a JEDEC-compliant IDT 4RCD0124KC0 RCD on the printed circuit board. Some modules have lower current requirements. Any specific module must meet the SDRAM and DDR4RCD01 voltage requirements for its worst case supply currents. *See, e.g.*, JEDEC RDIMM Standard (annotation added).  SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 81 (annotations added).

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

	Specifically, the SK hynix Products contain a IDT 4RCD0124KC0 RCD. (Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).  (Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD). (Exemplary Photo of SK Hynix HMA42GR7AFR4N-UHTD).

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

	The IDT 4RCD0124KC0 RCD is JEDEC Compliant. Features • JEDEC Compliant RCD *See* 4RCD0124K DDR4 Register Clock Driver Webpage at 1. **BENEFITS** • All devices are JEDEC® compliant and meet stringent requirements for reliability and application compliance IDT Leader in Server Memory Chipsets at 1. The SK hynix Products comprise a module controller coupled to the dynamic random access memory elements. For example, the IDT 4RCD0124KC0 RCD is coupled to the plurality of dynamic random access memory elements on the PCB.

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

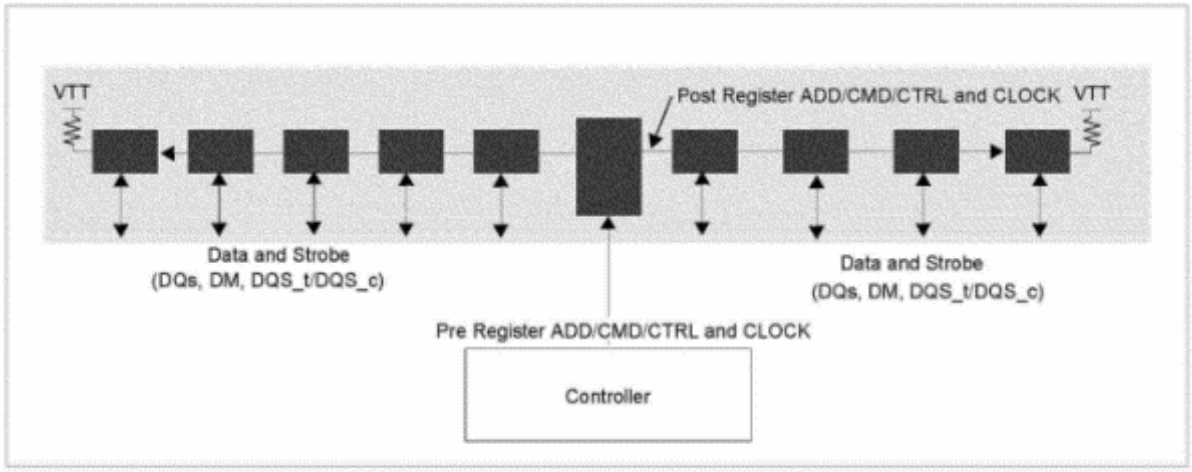


Figure 4 — Example RDIMM Topologies

JEDEC RDIMM Standard.

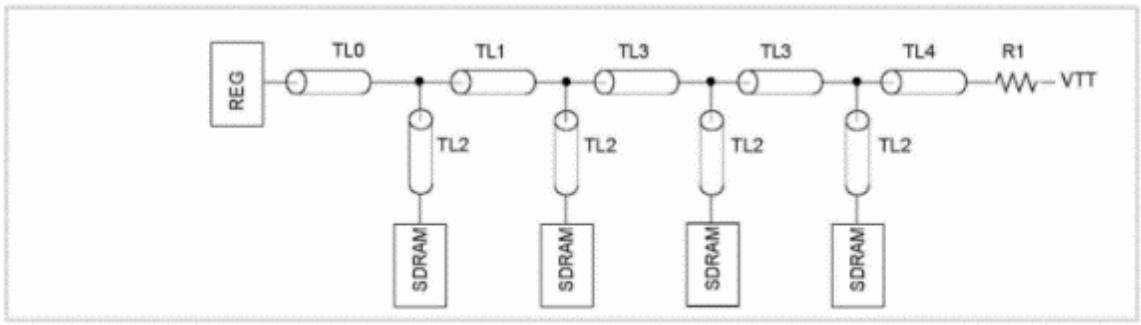
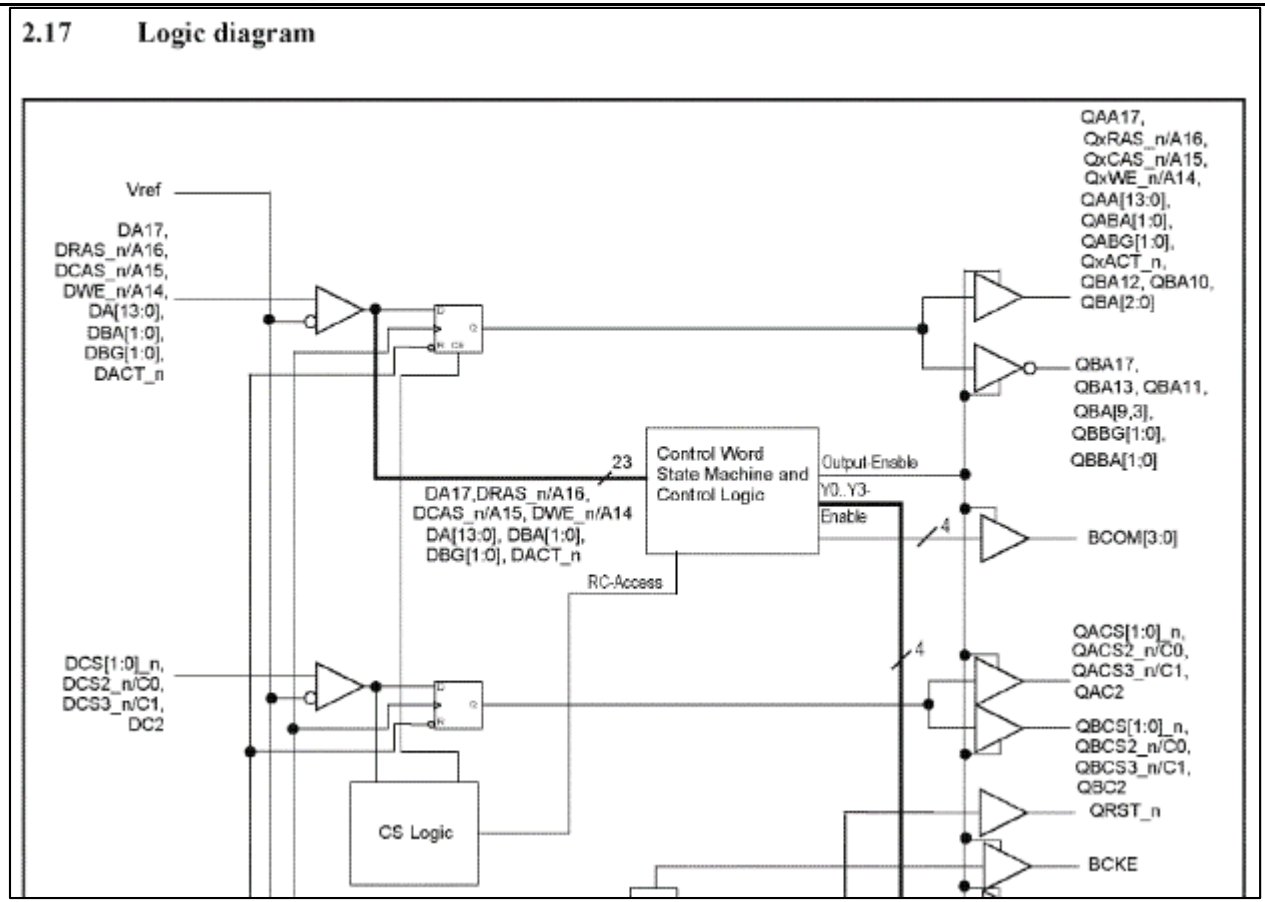


Figure 7 — Example PostRegister ADD/CMD Diagram

JEDEC RDIMM Standard.

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"



See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1 DODT0/1	CMOS[1] V_{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DCS0_n..DCS1_n	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals.
	DCS2_n..DCS3_n or DC0..DC1	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes,. Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
	DC2	CMOS[1] V_{REF} based	DRAM corresponding register Chip ID 2 signal.
Input Address and Command bus	DA0..DA13, DA17 DBA0..DBA1, DBG0..DBG1	CMOS[1] V_{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS[1] V_{REF} based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS[1] V_{REF} based	DRAM corresponding register DACT_n signal.

See JEDEC RCD01 Specification (annotations added).

Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS[2]	Register output CKE and ODT signals.
	QACS0_n..QACS1_n, QBCS0_n..QBCS1_n	CMOS[2]	Register output Chip Select signals.
	QACS2_n..QACS3_n, QBCS2_n..QBCS3_n or QAC0..QAC1, QBC0..QBC1	CMOS[2]	Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1
	QAC2, QBC2	CMOS[2]	Register output Chip ID2 signals.

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 10

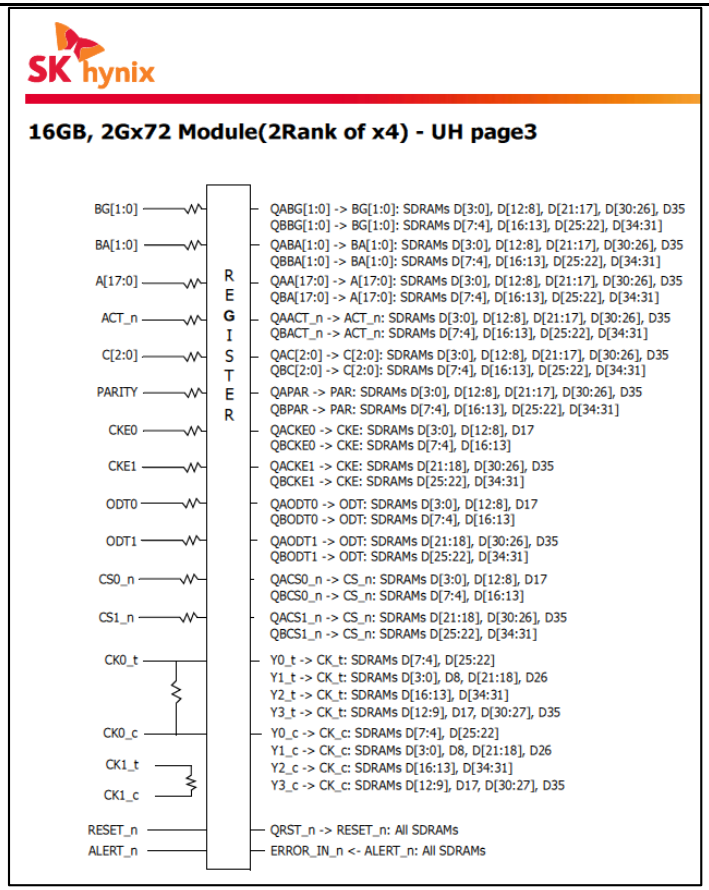
"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

Signal Group	Signal Name	Type	Description
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 10

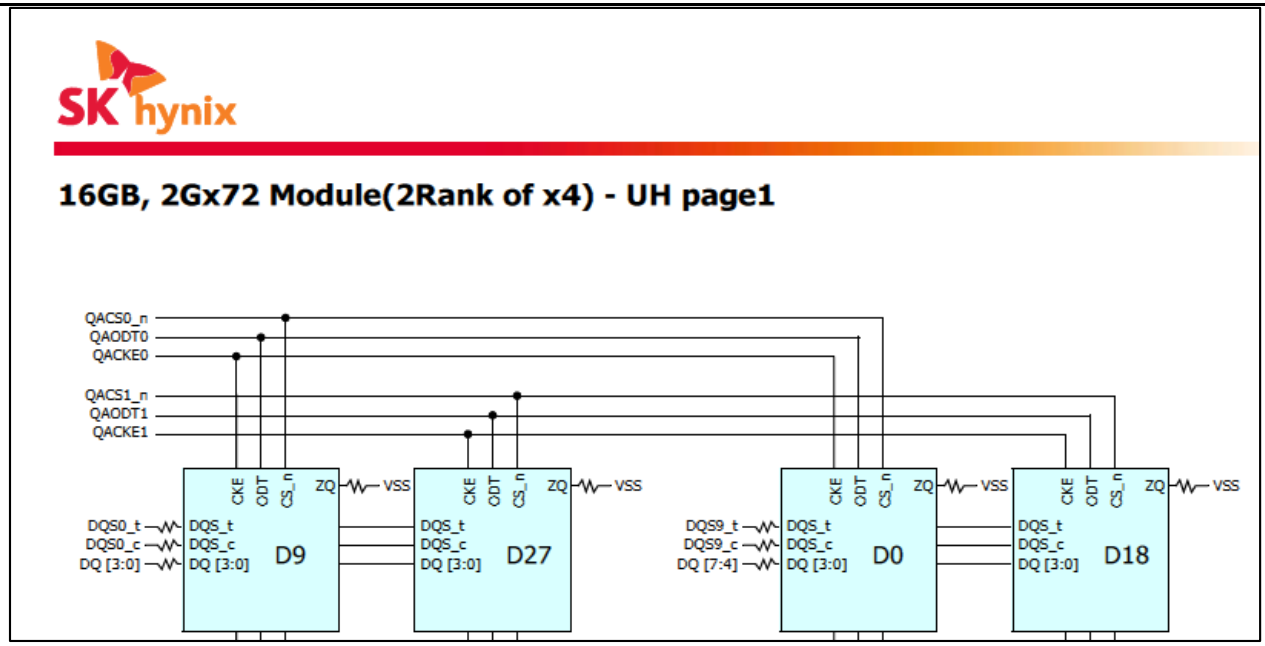
"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 22.

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 20.

The SK hynix Products comprise a module controller having an open drain output coupled to the error edge connection. For example, the JEDEC-complaint IDT 4RCD0124KC0 RCD contains an ALERT_n pin, which is an open drain output coupled to the error edge connection of the PCB.

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	$V_{DD}/2$	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS[2] differential	Redriven clock
Reset output	QRST_n	CMOS[2]	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR QBPAR	CMOS[2]	Redriven parity[3]
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I2C Register	SDA	Open drain I/O	I2C Bus Data

See JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

- CA Signals = QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2, QxPAR
- Control Signals = QxCKE0/1, QxODT0/1, QxC2, QxCS[1:0]_n for Dual CS mode, QxCS[3:0]
- CK = Yn_t - Yn_c

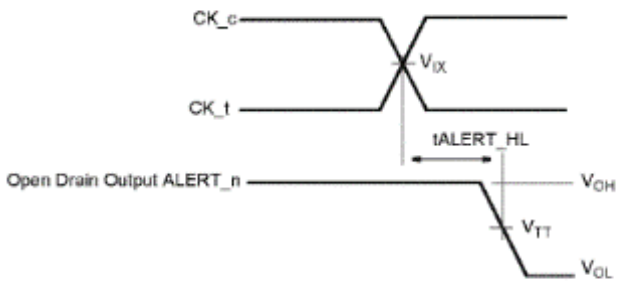


Figure 72 — Voltage waveforms, tALERT_HL Measurement

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I^2C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I^2C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I^2C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply

JEDEC RDIMM Standard (annotation added).

ALERT_n	Output (Input)	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system.

JEDEC RDIMM Standard (annotation added).

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 5, 7.

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

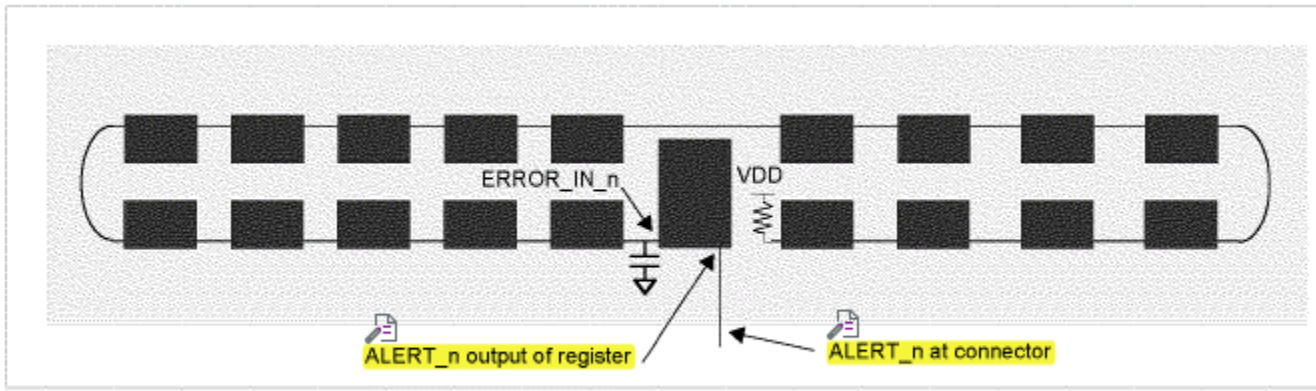
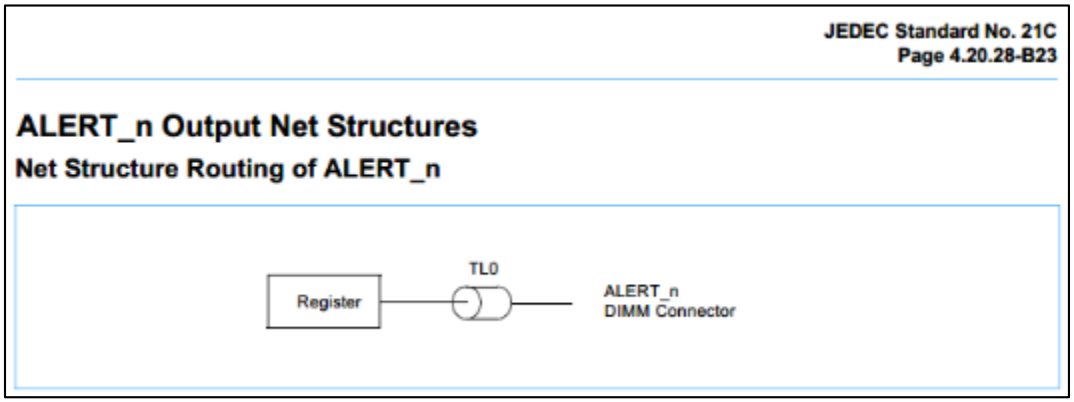


Figure 16 — Example Wiring of the ALERT_n Function

JEDEC RDIMM Standard (annotations added).



JEDEC Annex B- Raw Card B for RDIMM, at 20.

The module controller of the SK hynix Products is configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state. For example, the SK hynix products are configured to drive the Alert_n signal, from a HIGH state to a LOW state and from a LOW state to a HIGH state, while the memory module operates in the first mode (e.g., a normal mode of operation).

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I^2C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I^2C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I^2C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply

JEDEC RDIMM Standard (annotation added).

ALERT_n	Output (Input)	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system.

JEDEC RDIMM Standard (annotation added).

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 5, 7.

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

After the DDR4RCD01 receives DPAR from the memory controller, it compares it with the data received on the CA inputs and indicates on its open-drain ALERT_n pin (active LOW) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[n:0]_n signals being LOW.

The convention of parity is even parity, i.e., valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even. The DIMM-dependent control signals (DCKE0, DCKE1, DCS0_n .. DCS3_n, DODT0 and DODT1) are not included in the parity check computations.

Even after a CA parity error has been registered, the device will still forward DCKEn and DODTn to the DRAMs, and the device will enter CKE power down mode depending on the DCKEn transitions.

If a parity error occurs and parity checking is enabled in RC0E, the DDR4 register sets the 'CA Parity Error Status' bit in RCFx to '1'and disables parity checking. ALERT_n is asserted three input clocks after the erroneous command is registered. If the 'CA Parity Error Status' bit is '0', the DDR4 register logs the error by storing the erroneous command and address bits in the Error Log Register. ALERT_n stays asserted LOW until a 'Clear CA Parity Error Status' command is sent if the 'ALERT_n Assertion' bit in the Parity Control Word (RC0E) is '0'. In this case the erroneous command and all subsequent commands

See, e.g., JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

2.18 Control Words

The device features a set of control words, which allow the optimization of the device properties for different raw card designs. DDR4RCD01 control word (RCW) writes appear like DRAM MRS commands to MR7 which are ignored by the DDR4 DRAM. Each RCW write generates an MRS command to the rank 0 DRAMs behind the register, unless there is a parity error when parity checking is enabled, in which case both the RCW write as well as the MRS command to the DRAM are blocked. The different control words and settings are described below. Any change to these control words require some time for the device to settle. For changes to the control word setting, except for RC02 (DA3) and RC0A/RC3x, the controller needs to wait t_{MRD} after the last control word access, before further access to the DRAM can take place. For any changes to the clock timing (RC02: bit DA3, and RC0A/RC3x) this settling may take up to tSTAB time. All chip select inputs, DCS[n:0]_n, must be kept HIGH during that time.

The DDR4RCD01 allocates decoding for up to 16 4-bit words of control bits (RC00 through RC0F) and up to 15 8-bit words of control bits. Selection of each word of 4-bit control bits is presented on inputs DA4 through DA12. Data to be written into the 4-bit configuration registers need to be presented on DA0 .. DA3. Selection of each word of 8-bit control bits is presented on inputs DA8 through DA12. Data to be written into the 8-bit configuration registers need to be presented on DA0 .. DA7. Bits DA[16:14] must be LOW and at least one DCKEn input must be HIGH for a valid access. If register CKE power down feature is disabled, DCKEn inputs are don't care (either HIGH or LOW), and are forwarded to the QxCKEn outputs. The DODT[1:0] inputs are also don't care (can be either HIGH or LOW), and are forwarded to the QxODT[1:0] outputs. Address and command parity is checked during control word write operations unless parity is disabled in the Parity Control Word. ALERT_n is asserted and the command is ignored if a parity error is detected.

See JEDEC RCD01 Specification (annotations added).

Additionally, for example, the SK hynix Products are configured to drive the Alert_n signal, from a HIGH state to a LOW state and from a LOW state to a HIGH state, while the memory module is in Clock-to-CA training mode, e.g., the second mode.

U.S. Patent No. 10,474,595: Claim 10

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2.12 CA Bus Training Modes

The DDR4RCD01 supports several training modes (selected in Table 35, "RC0C: Training Control Word") in order to assist the memory controller in aligning the incoming command/address and control signals optimally to the input clock signal CK_t/CK_t. These training modes are only available if a non-zero latency adder has been selected.

In Clock-to-CA training mode the DDR4RCD01 ORs all enabled Dn inputs[1] every other cycle together and loops back the result to the ALERT_n output pin. In this mode, the DPAR input is sampled at the same time as the other Dn inputs. The ALERT_n latency relative to the DQn inputs is the same 3 cycles as in the normal parity mode. During any of the CA bus training modes, QCA/QxCKEn and QxODTn hold their previous values and parity checking is disabled.

The memory controller can use the Clock-to-CA training mode and feedback from the DDR4RCD01 to adjust the CK_t-CK_c to Dn relationship analogous to the write leveling sequence which adjusts the DQS-DQS_n to CK_t-CK_c relationship. The memory controller writes consecutive sequences of all '1's and all '0's on the CA bus and pulls in the Dn timing until the DDR4RCD01 samples all Dn inputs as 0, which is indicated with the LOW assertion of ALERT_n. This position indicates the start position of a cumulative CA bus "eye opening". The memory controller advances the clock position or pulls in the Dn timing until the DDR4RCD01 samples at least one input as '1', which is indicated by ALERT_n remaining high three cycles after the last command. This position indicates the end position of a cumulative CA bus "eye opening". The memory controller can now position either the clock phase or the Dn input timing so that the clock edge is in the middle of this "eye opening" to achieve equal amounts of setup and hold time relative to the clock edge.

Figure 22 shows three sampling phase positions where the loopback ALERT_n pin transmits either a consistent 0 output, a randomly toggling 1/0 output or a consistent 1 output, indicating sampling positions at the LOW time, the transition time or the HIGH time of the inputs, respectively.

The memory controller can use the DCS0_n, DCS1_n, DCKE0, DCKE1, DODT0 and DODT0 loop back modes in similar fashion. In each of these modes a single input signal is looped back to the ALERT_n output and the memory controller can determine the optimal clock position for each of the control signals that are used for a particular DIMM. Once the optimal clock position for all CMD/ADDR and control inputs has been established, the memory controller can determine the best clock position for the whole set of input signals or potentially move the timing of individual control signals around to increase either setup or hold margins relative to the clock edge.

See JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

- CA Signals = QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2, QxPAR
- Control Signals = QxCKE0/1, QxODT0/1, QxC2, QxCS[1:0]_n for Dual CS mode, QxCS[3:0]
- CK = Yn_t - Yn_c

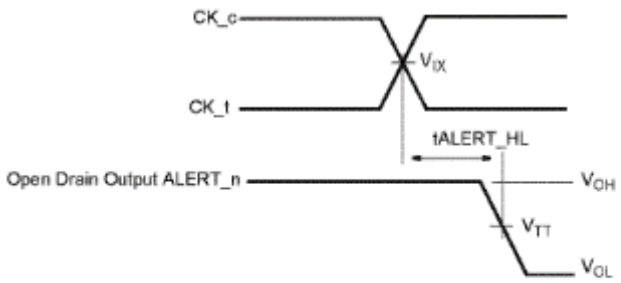

Figure 72 — Voltage waveforms, tALERT_HL Measurement

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	$V_{DD}/2$	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS[2] differential	Redriven clock
Reset output	QRST_n	CMOS[2]	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR QBPAR	CMOS[2]	Redriven parity[3]
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I2C Register	SDA	Open drain I/O	I2C Bus Data

See JEDEC RCD01 Specification (annotation added).

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

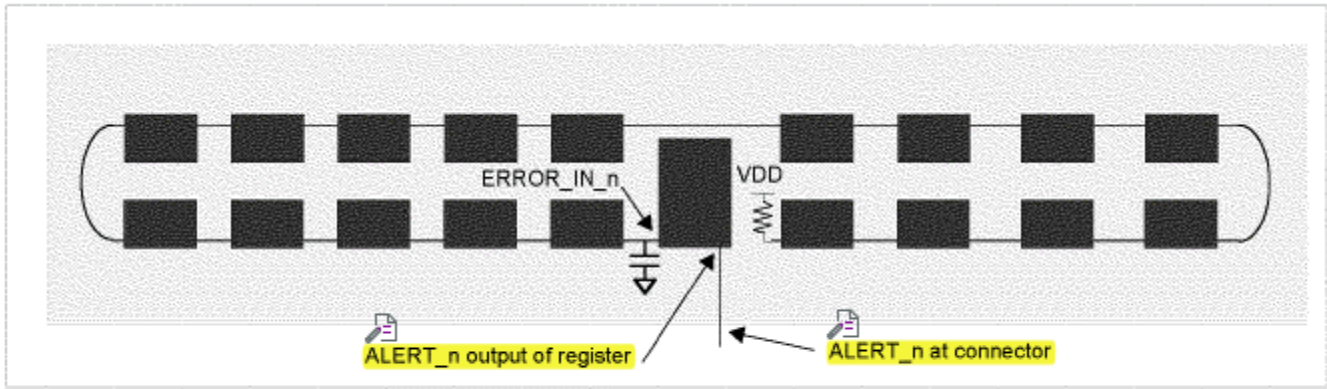

Figure 16 — Example Wiring of the ALERT_n Function

JEDEC RDIMM Standard (annotations added).

The Alert_n signal provides information related to the one or more training sequences. For example, while in Clock-to-CA training mode, the IDT 4RCD0124KC0 RCD ORs all enabled Dn inputs from the memory controller and then outputs the result of that OR operation to the memory controller via the Alert_n pin. The module controller of the SK hynix Products drives the open drain output and the error edge connection to one of two states.

U.S. Patent No. 10,474,595: Claim 10

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2.12 CA Bus Training Modes

The DDR4RCD01 supports several training modes (selected in Table 35, "RC0C: Training Control Word") in order to assist the memory controller in aligning the incoming command/address and control signals optimally to the input clock signal CK_t/CK_t. These training modes are only available if a non-zero latency adder has been selected.

In Clock-to-CA training mode the DDR4RCD01 ORs all enabled Dn inputs[1] every other cycle together and loops back the result to the ALERT_n output pin. In this mode, the DPAR input is sampled at the same time as the other Dn inputs. The ALERT_n latency relative to the DQn inputs is the same 3 cycles as in the normal parity mode. During any of the CA bus training modes, QCA/QxCKEn and QxODTn hold their previous values and parity checking is disabled.

The memory controller can use the Clock-to-CA training mode and feedback from the DDR4RCD01 to adjust the CK_t-CK_c to Dn relationship analogous to the write leveling sequence which adjusts the DQS-DQS_n to CK_t-CK_c relationship. The memory controller writes consecutive sequences of all '1's and all '0's on the CA bus and pulls in the Dn timing until the DDR4RCD01 samples all Dn inputs as 0, which is indicated with the LOW assertion of ALERT_n. This position indicates the start position of a cumulative CA bus "eye opening". The memory controller advances the clock position or pulls in the Dn timing until the DDR4RCD01 samples at least one input as '1', which is indicated by ALERT_n remaining high three cycles after the last command. This position indicates the end position of a cumulative CA bus "eye opening". The memory controller can now position either the clock phase or the Dn input timing so that the clock edge is in the middle of this "eye opening" to achieve equal amounts of setup and hold time relative to the clock edge.

Figure 22 shows three sampling phase positions where the loopback ALERT_n pin transmits either a consistent 0 output, a randomly toggling 1/0 output or a consistent 1 output, indicating sampling positions at the LOW time, the transition time or the HIGH time of the inputs, respectively.

The memory controller can use the DCS0_n, DCS1_n, DCKE0, DCKE1, DODT0 and DODT0 loop back modes in similar fashion. In each of these modes a single input signal is looped back to the ALERT_n output and the memory controller can determine the optimal clock position for each of the control signals that are used for a particular DIMM. Once the optimal clock position for all CMD/ADDR and control inputs has been established, the memory controller can determine the best clock position for the whole set of input signals or potentially move the timing of individual control signals around to increase either setup or hold margins relative to the clock edge.

See JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 10

"a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and"

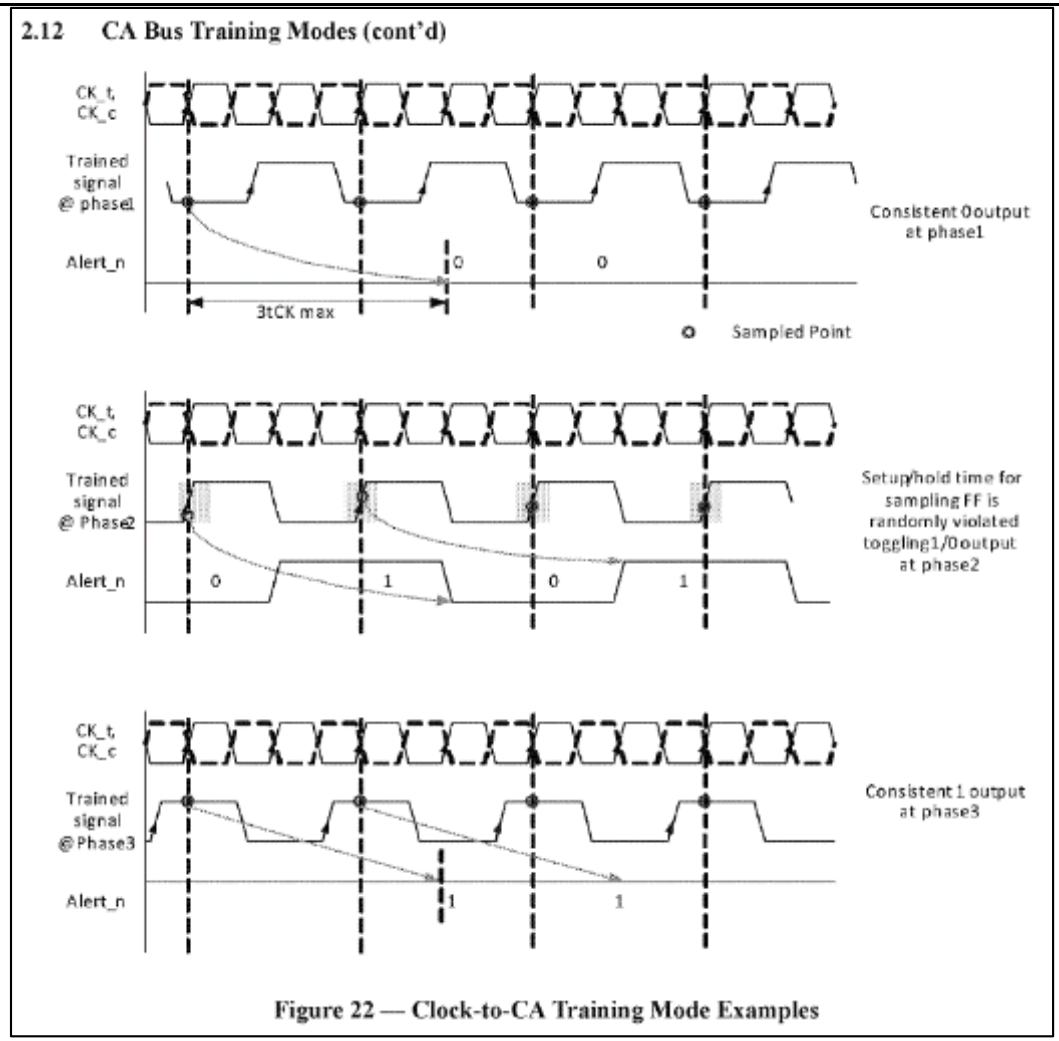


Figure 22 — Clock-to-CA Training Mode Examples

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 10

"wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections"

wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections	The SK hynix Products are operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections. For example, the SK hynix Product is configured to operate in a first mode, e.g., a normal operating mode (e.g., when the IDT 4RCD0124KC0 RCD's RC0C control word = x000), and in a second mode, e.g., Clock-to-CA training mode (e.g., when the IDT 4RCD0124KC0 RCD's RC0C control word = x001). **Table 35 — RC0C: Training Control Word** **Setting (DA[3:0])** / **Definition** / **Encoding** x 0 0 0 — Training mode selection — Normal operating mode x 0 0 1 — Clock-to-CA training mode[1] x 0 1 0 — DCS0_n loopback mode[1] x 0 1 1 — DCS1_n loopback mode[1] x 1 0 0 — DCKE0 loopback mode[1] x 1 0 1 — DCKE1 loopback mode[1] x 1 1 0 — DODT0 loopback mode[1] x 1 1 1 — DODT1 loopback mode[1] 0 x x x — Reserved — Reserved 1 x x x — Reserved 1. In these training modes the DDR4RCD01 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals). *See* JEDEC RCD01 Specification (annotations added). For example, the IDT 4RCD0124KC0 RCD is further configured to operate in a second mode, e.g., Clock-to-CA training mode (e.g., when RC0C control word = x001).

U.S. Patent No. 10,474,595: Claim 10

"wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections"

Table 35 — RC0C: Training Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	Training mode selection	Normal operating mode
x	0	0	1		Clock-to-CA training mode[1]
x	0	1	0		DCS0_n loopback mode[1]
x	0	1	1		DCS1_n loopback mode[1]
x	1	0	0		DCKE0 loopback mode[1]
x	1	0	1		DCKE1 loopback mode[1]
x	1	1	0		DODT0 loopback mode[1]
x	1	1	1		DODT1 loopback mode[1]
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

1. In these training modes the DDR4RCD01 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals).

See JEDEC RCD01 Specification (annotations added).

The SK hynix Products are operable in a first mode (e.g., a normal operation mode) in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections.

Table 35 — RC0C: Training Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	Training mode selection	Normal operating mode
x	0	0	1		Clock-to-CA training mode[1]
x	0	1	0		DCS0_n loopback mode[1]
x	0	1	1		DCS1_n loopback mode[1]
x	1	0	0		DCKE0 loopback mode[1]
x	1	0	1		DCKE1 loopback mode[1]
x	1	1	0		DODT0 loopback mode[1]
x	1	1	1		DODT1 loopback mode[1]
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

1. In these training modes the DDR4RCD01 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals).

See JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 10

"wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections"

	The SK hynix Products are configured to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections. For example, during the first mode (e.g., a normal mode of operation), the RCD receives address and control signals corresponding to read and write commands from the memory controller via the second edge connections. The RCD outputs corresponding address and control signals to the SDRAM devices, which cause the SDRAM devices to execute read and write operations. Additionally, the RCD outputs chips select commands QACS0_n, QACS1_N, and/or QACS3_n, and QBCS0_n, QBCS1_N, and/or QBCS3_n, which activate the relevant SDRAM chip depending on the mode of operation. **2.2 Features and Functions** The DDR4RCD01 has three basic modes of operation associated with the DA[1:0] bits in the DIMM Configuration Control Word (RC0D): • In **Direct DualCS mode** (DA[1:0] = 00) the component has two chip select inputs, DCS0_n and DCS1_n, and two copies of each chip select output, QACS0_n, QACS1_n, QBCS0_n and QBCS1_n. The inputs pins DC[2:0] are forwarded to two sets of output pins, QAC[2:0] and QBC[2:0]. This is the normal operating mode ("QuadCS disabled" and "Encoded CS disabled"). • In **Direct QuadCS mode** (DA[1:0] = 01), the component has four chip select inputs, the two dedicated inputs DCS[1:0]_n and the DC[0] input pin functioning as DCS2_n and the DC[1] input pin functioning as DCS3_n, and two copies of each chip select output, QACS[3:0]_n and QBCS[3:0]_n. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "QuadCS enabled" mode. In the two modes above the DDR4 register does not need to decode input signals to generate any chip select outputs. • In **Encoded QuadCS mode** (DA[1:0] = 11), two copies of four output chip selects, i.e., QACS[3:0]_n and QBCS[3:0]_n, are decoded out of two DCS[1:0]_n inputs and the DC[0] input. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "Encoded QuadCS" mode. *See* JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 10

"wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections"

In response to the address and command information received via the second edge connections, the SK hynix Products perform one or more memory read or write operations by communicating data signals via the first edge connections. For example the DQ and DQS signals (first edge connections) are used to communicate data signals between the memory module and host in response to read/write commands and addressing information received from the second edge connections:

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I^2C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I^2C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I^2C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS9_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	DM0_n-DM8_n	Data Mask
DQS0_c-DQS17_c	Data Buffer data strobes	RESET_n	Set Register and SDRAMs to a Known State

DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.

U.S. Patent No. 10,474,595: Claim 10

"wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections"

DQS0_t-DQS17_t, DQS0_c-DQS17_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

JEDEC RDIMM Standard.

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 5, 7.

6 DIMM Design Details

6.1 Signal Groups

This specification categorizes DDR4 SDRAM signals into six groups. Figure 4 illustrates the DIMM wiring. All signal groups, except DQ, implement a fly-by topology.

The signal groups are:

1. DQ and DQS signals connector to SDRAM

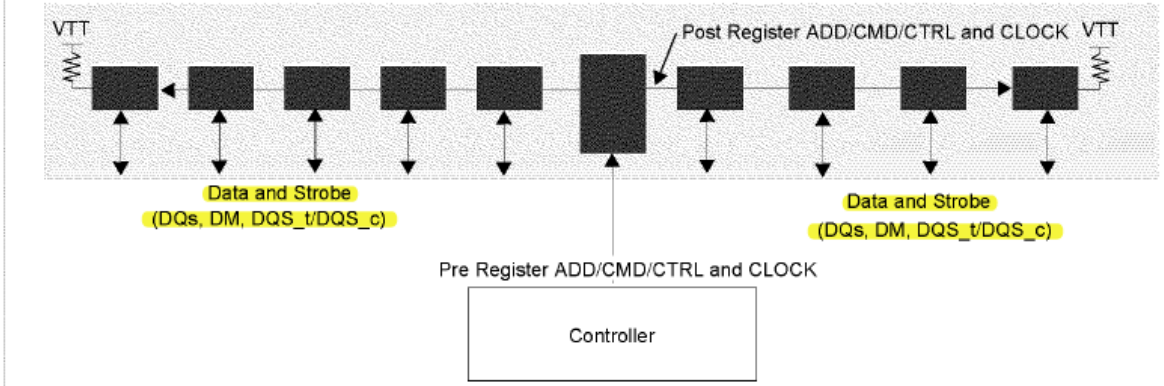


Figure 4 — Example RDIMM Topologies

U.S. Patent No. 10,474,595: Claim 10

"wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections"

JEDEC RDIMM Standard (annotations added).

> Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

JEDEC DDR4 SDRAM Specification (annotations added).

See also SKH DDR4 Device Operation at 7.

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

JEDEC DDR4 SDRAM Specification (annotations added).

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 7.

U.S. Patent No. 10,474,595: Claim 10

"wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections"

JEDEC Standard No. 79-4A
Page 86

4.24.1.2 READ Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 67 and is applied when the DLL is enabled and locked.

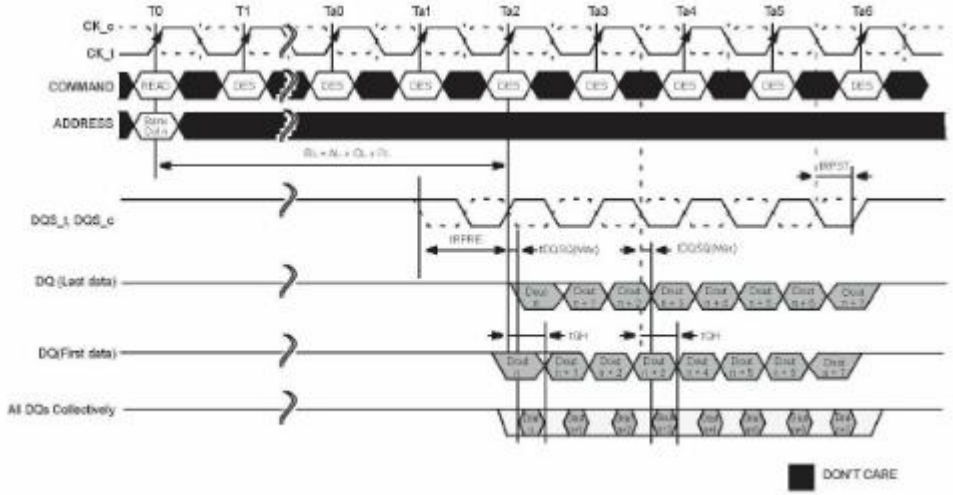
Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

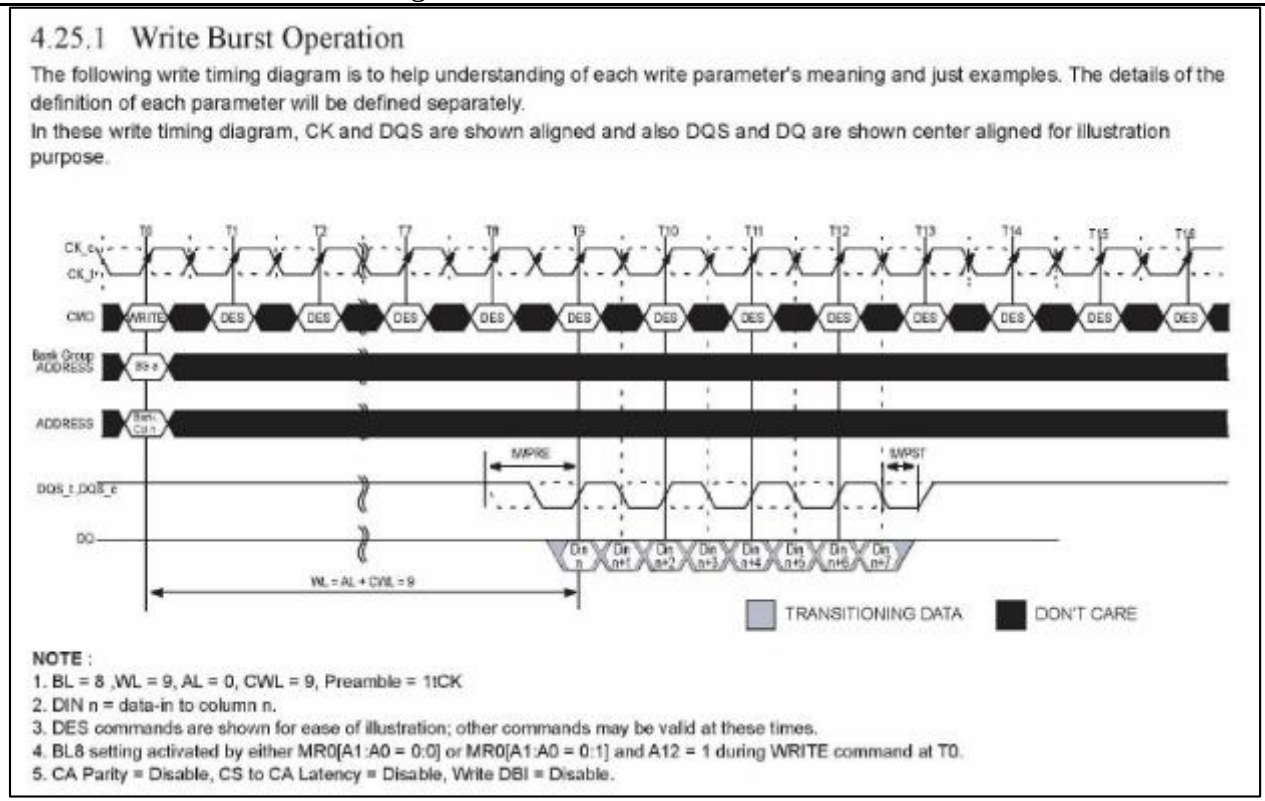
tDQSQ: both rising/falling edges of DQS, no tAC defined.



See, e.g., JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 97.

U.S. Patent No. 10,474,595: Claim 10

"wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections"



See, e.g., JEDEC DDR4 SDRAM Specification.
See also JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 126, 94-144.

In the second mode, the SK hynix Products are not accessed by the memory controller for normal memory read or write operations, and are configurable to perform operations related to one or more training sequences.

For example, while the SK hynix Product is in Clock-to-CA training mode (e.g., a second mode), the dynamic random access memory devices (DRAMs) of the memory module are isolated from normal use, and normal operational read/write commands are not decoded.

U.S. Patent No. 10,474,595: Claim 10

"wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections"

	The DRAM is protected by driving the RCD control outputs at inactive levels. The RCD may either force all outputs than can be chip selects (including QxC0/CS2_n and QxC1/CS3_n) HIGH and all QxCKE and QxODT outputs LOW OR hold the previous values on QxCA/QxCS/QxCKE/QxODT before entering any of the CA training modes. The data buffer is protected by driving the buffer control interface signals at inactive levels. The RCD may either drive BODT and BCKE outputs LOW and BCOM[3:0] to '1010' (NOP command) OR the RCD may hold the previous values on BODT/BCKE/BCOM before entering any of the CA training modes. The RCD does not decode commands while any RC0C training mode is enabled. It is thus necessary for the register to correspondingly disable and ignore unused inputs in each training mode. The following two methods to change or exit CA training modes are supported: (a) Write access to RC0C through I^2C Bus and (b) DRST_n Reset event. *See* JEDEC RCD01 Specification. Further, while in the second mode, the SK hynix Products are configurable to perform operations related to one or more training sequences.

U.S. Patent No. 10,474,595: Claim 10

"wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections"

2.12 CA Bus Training Modes

The DDR4RCD01 supports several training modes (selected in Table 35, "RC0C: Training Control Word") in order to assist the memory controller in aligning the incoming command/address and control signals optimally to the input clock signal CK_t/CK_t. These training modes are only available if a non-zero latency adder has been selected.

In Clock-to-CA training mode the DDR4RCD01 ORs all enabled Dn inputs[1] every other cycle together and loops back the result to the ALERT_n output pin. In this mode, the DPAR input is sampled at the same time as the other Dn inputs. The ALERT_n latency relative to the DQn inputs is the same 3 cycles as in the normal parity mode. During any of the CA bus training modes, QCA/QxCKEn and QxODTn hold their previous values and parity checking is disabled.

The memory controller can use the Clock-to-CA training mode and feedback from the DDR4RCD01 to adjust the CK_t-CK_c to Dn relationship analogous to the write leveling sequence which adjusts the DQS-DQS_n to CK_t-CK_c relationship. The memory controller writes consecutive sequences of all '1's and all '0's on the CA bus and pulls in the Dn timing until the DDR4RCD01 samples all Dn inputs as 0, which is indicated with the LOW assertion of ALERT_n. This position indicates the start position of a cumulative CA bus "eye opening". The memory controller advances the clock position or pulls in the Dn timing until the DDR4RCD01 samples at least one input as '1', which is indicated by ALERT_n remaining high three cycles after the last command. This position indicates the end position of a cumulative CA bus "eye opening". The memory controller can now position either the clock phase or the Dn input timing so that the clock edge is in the middle of this "eye opening" to achieve equal amounts of setup and hold time relative to the clock edge.

Figure 22 shows three sampling phase positions where the loopback ALERT_n pin transmits either a consistent 0 output, a randomly toggling 1/0 output or a consistent 1 output, indicating sampling positions at the LOW time, the transition time or the HIGH time of the inputs, respectively.

The memory controller can use the DCS0_n, DCS1_n, DCKE0, DCKE1, DODT0 and DODT0 loop back modes in similar fashion. In each of these modes a single input signal is looped back to the ALERT_n output and the memory controller can determine the optimal clock position for each of the control signals that are used for a particular DIMM. Once the optimal clock position for all CMD/ADDR and control inputs has been established, the memory controller can determine the best clock position for the whole set of input signals or potentially move the timing of individual control signals around to increase either setup or hold margins relative to the clock edge.

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 10

"wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections"

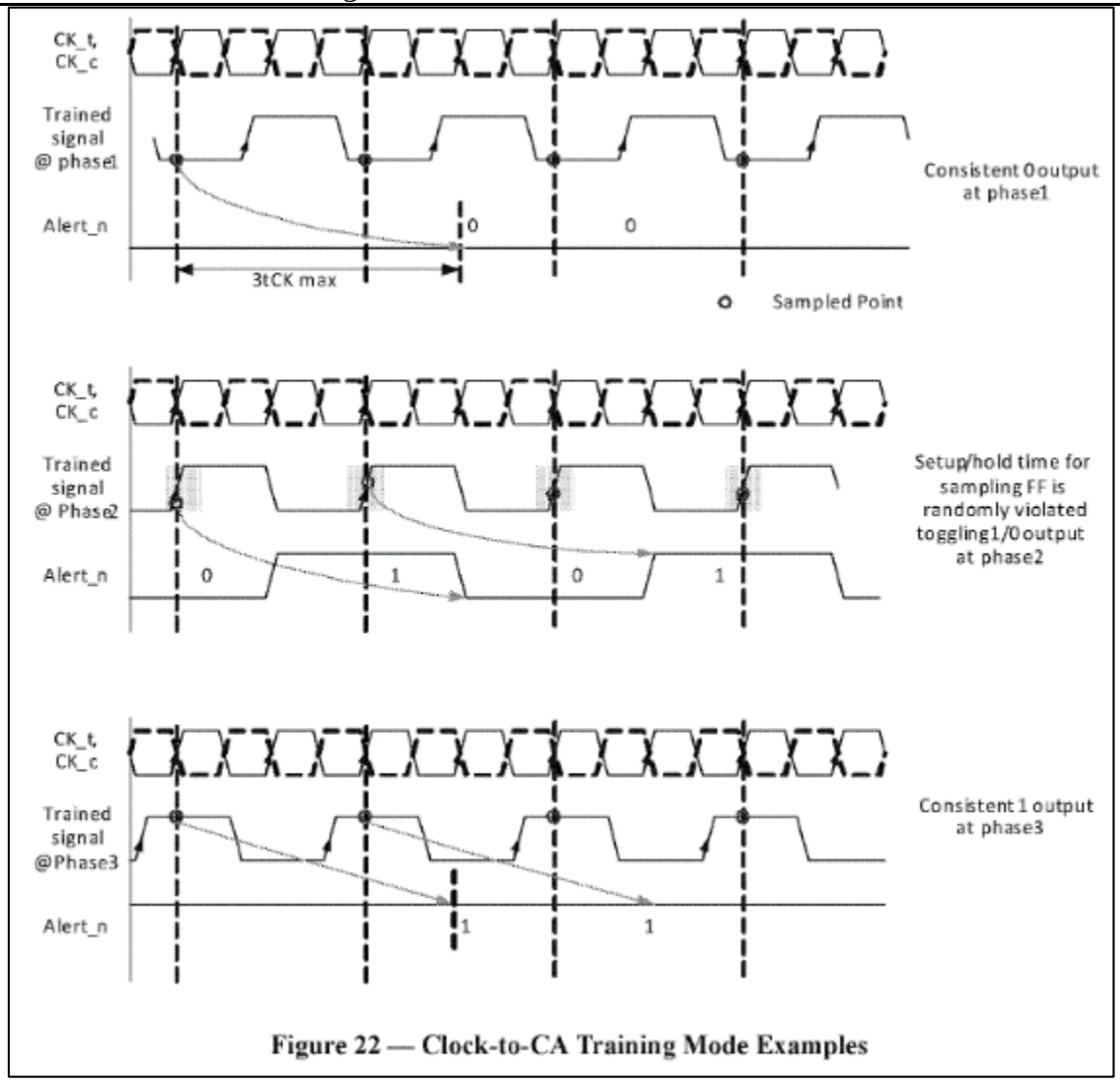


Figure 22 — Clock-to-CA Training Mode Examples

See JEDEC RCD01 Specification.

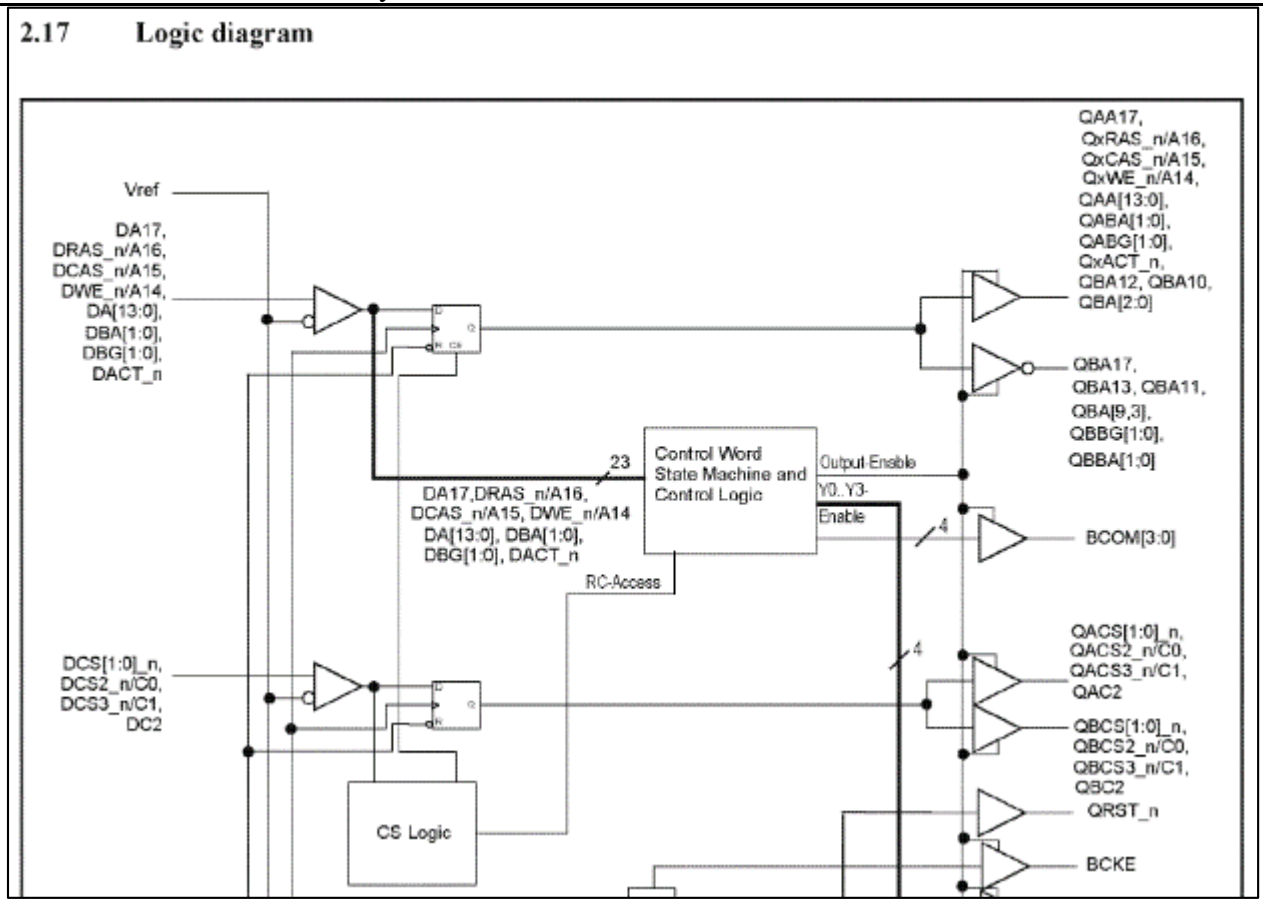
U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;	The module controller of the SK hynix Products is, in the first mode, configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals. The module controller of the SK hynix Products is further configurable, in the first mode, to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module. While the SK hynix Products are in the first mode, the module controller of the SK hynix Products is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations. For example, during the first mode (e.g., a normal mode of operation), the RCD receives address and control signals corresponding to read and write commands from the memory controller via the second edge connections.

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

	2.17 Logic diagram  *See* JEDEC RCD01 Specification.

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1 DODT0/1	CMOS[1] V_{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DCS0_n..DCS1_n	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals.
	DCS2_n..DCS3_n or DC0..DC1	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes,. Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
	DC2	CMOS[1] V_{REF} based	DRAM corresponding register Chip ID 2 signal.
Input Address and Command bus	DA0..DA13, DA17 DBA0..DBA1, DBG0..DBG1	CMOS[1] V_{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS[1] V_{REF} based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS[1] V_{REF} based	DRAM corresponding register DACT_n signal.

See JEDEC RCD01 Specification (annotations added).

Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS[2]	Register output CKE and ODT signals.
	QACS0_n..QACS1_n, QBCS0_n..QBCS1_n	CMOS[2]	Register output Chip Select signals.
	QACS2_n..QACS3_n, QBCS2_n..QBCS3_n or QAC0..QAC1, QBC0..QBC1	CMOS[2]	Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1
	QAC2, QBC2	CMOS[2]	Register output Chip ID2 signals.

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 10

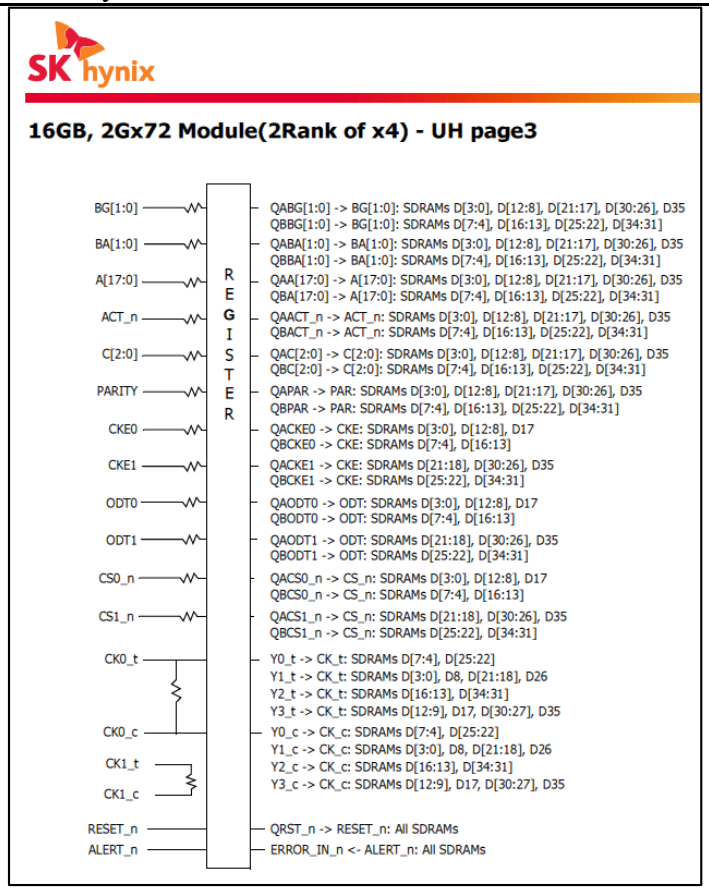
"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

Signal Group	Signal Name	Type	Description
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 10

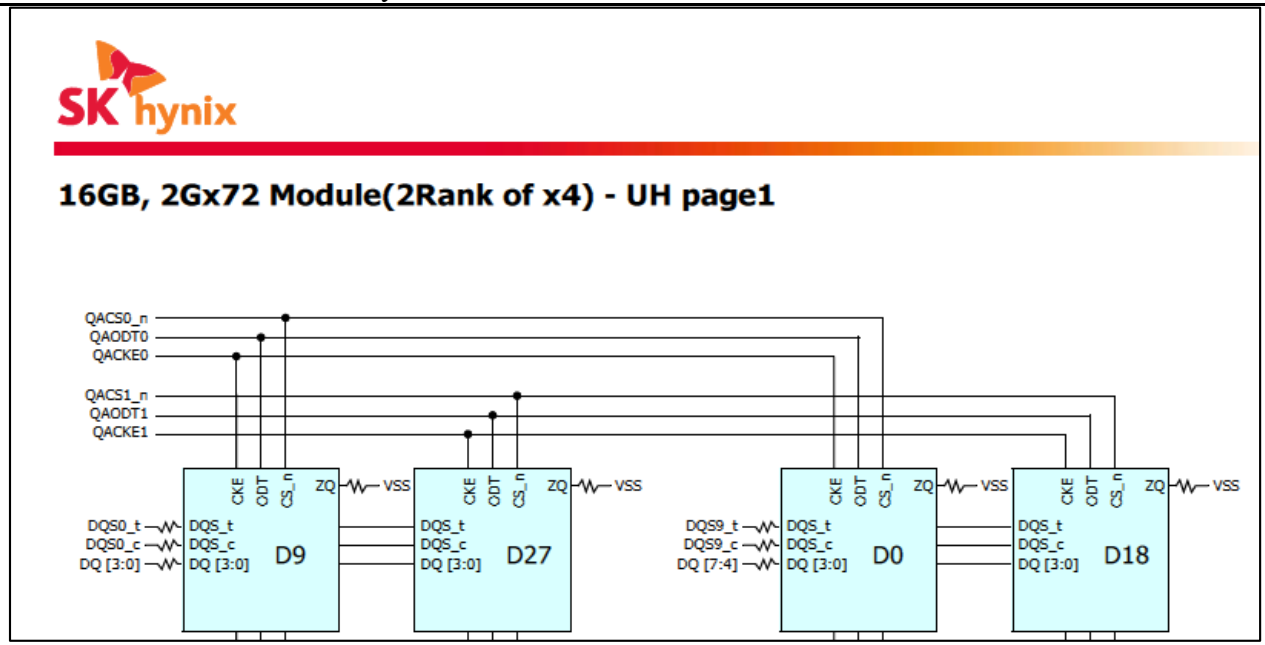
"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 22.

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"



SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 20.

Further, in the first mode, the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals. For example, the RCD outputs the address and control signals to the SDRAM devices, which cause the SDRAM devices to execute read and write operations. The SDRAM components receive these signals as inputs from the RCD.

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

2.6 Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code

JEDEC DDR4 SDRAM Specification.

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 6.

RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table

JEDEC DDR4 SDRAM Specification.

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 6.

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.

JEDEC DDR4 SDRAM Specification.

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 6.

These signals are used during reads and writes that occur during the normal operational mode, e.g., the first mode.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner.

JEDEC DDR4 SDRAM Specification (annotations added).
See also SKH DDR4 Device Operation at 7.

4.22 ACTIVATE Command

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BG0-BG1 in X4/8 and BG0 in X16 select the bankgroup; BA0-BA1 inputs selects the bank within the bankgroup, and the address provided on inputs A0-A17 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank or a precharge all command is issued. A bank must be precharged before opening a different row in the same bank.

JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 94.

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

Additionally, the RCD outputs chips select commands QACS0_n, QACS1_N, and/or QACS3_n, and QBCS0_n, QBCS1_N, and/or QBCS3_n, which activate the relevant SDRAM chip depending on the mode of operation.

2.2 Features and Functions

The DDR4RCD01 has three basic modes of operation associated with the DA[1:0] bits in the DIMM Configuration Control Word (RC0D):

- In **Direct DualCS mode** (DA[1:0] = 00) the component has two chip select inputs, DCS0_n and DCS1_n, and two copies of each chip select output, QACS0_n, QACS1_n, QBCS0_n and QBCS1_n. The inputs pins DC[2:0] are forwarded to two sets of output pins, QAC[2:0] and QBC[2:0]. This is the normal operating mode ("QuadCS disabled" and "Encoded CS disabled").
- In **Direct QuadCS mode** (DA[1:0] = 01), the component has four chip select inputs, the two dedicated inputs DCS[1:0]_n and the DC[0] input pin functioning as DCS2_n and the DC[1] input pin functioning as DCS3_n, and two copies of each chip select output, QACS[3:0]_n and QBCS[3:0]_n. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "QuadCS enabled" mode.

  In the two modes above the DDR4 register does not need to decode input signals to generate any chip select outputs.
- In **Encoded QuadCS mode** (DA[1:0] = 11), two copies of four output chip selects, i.e., QACS[3:0]_n and QBCS[3:0]_n, are decoded out of two DCS[1:0]_n inputs and the DC[0] input. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "Encoded QuadCS" mode.

See JEDEC RCD01 Specification.

In accordance with those address and control signals, the SDRAM communicate data signals with the memory controller via the first edge connections. For example the DQ and DQS signals (first edge connections) are used to communicate data signals between the memory module and host in response to read/write commands and addressing information received from the second edge connections:

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I^2C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I^2C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I^2C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS9_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	DM0_n-DM8_n	Data Mask
[illegible]	Data Buffer data strobes	[illegible]	[illegible]

DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.

DQS0_t-DQS17_t, DQS0_c-DQS17_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

JEDEC RDIMM Standard.

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 5, 7.

6 DIMM Design Details

6.1 Signal Groups

This specification categorizes DDR4 SDRAM signals into six groups. Figure 4 illustrates the DIMM wiring. All signal groups, except DQ, implement a fly-by topology.

The signal groups are:

1. DQ and DQS signals connector to SDRAM

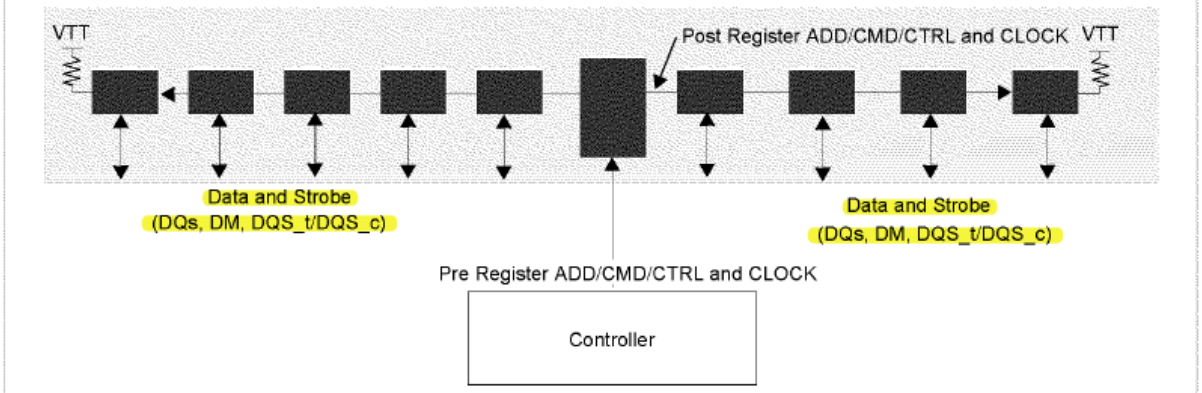


Figure 4 — Example RDIMM Topologies

JEDEC RDIMM Standard (annotations added).

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

	Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register. JEDEC DDR4 SDRAM Specification (annotations added). *See also* SKH DDR4 Device Operation at 7. **Symbol** | **Type** | **Function** DQ | Input / Output | Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used. DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c | Input / Output | Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended. JEDEC DDR4 SDRAM Specification (annotations added). *See also* SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 7.

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

JEDEC Standard No. 79-4A
Page 86

4.24.1.2 READ Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 67 and is applied when the DLL is enabled and locked.

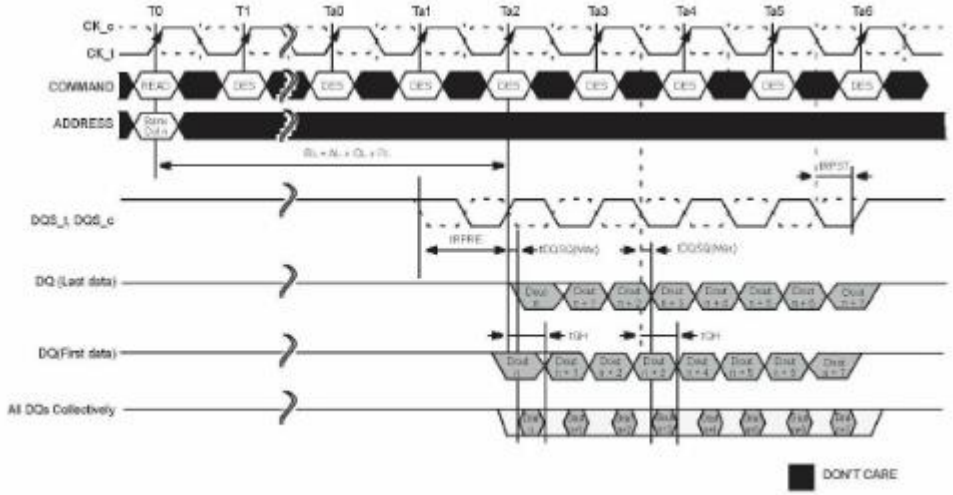
Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

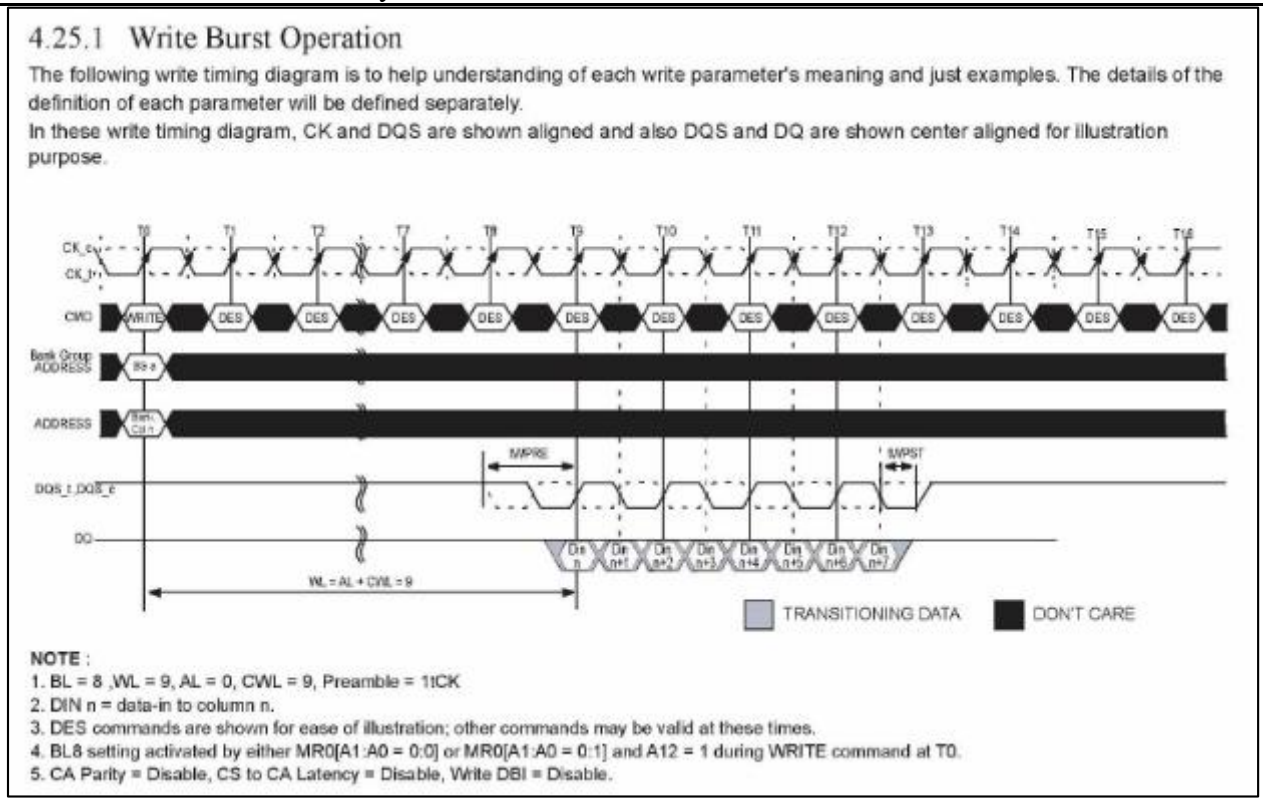
tDQSQ: both rising/falling edges of DQS, no tAC defined.



See, e.g., JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 97.

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"



4.25.1 Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.

In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.

NOTE :
1. BL = 8 ,WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

See, e.g., JEDEC DDR4 SDRAM Specification.
See also JEDEC DDR4 SDRAM Specification.
See also SKH DDR4 Device Operation at 126, 94-144.

The module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the SK hynix Products are in the first mode. For example, the ALERT_n pin of the SK hynix Products is used to indicate a parity error while the memory module operates in the first mode (e.g., a normal mode of operation).

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I^2C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I^2C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I^2C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply

JEDEC RDIMM Standard (annotation added).

ALERT_n	Output (Input)	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system.

JEDEC RDIMM Standard (annotation added).

See also SKH HHMA451R7AFR8N / HMA41GR7AFR8N / HMA41GR7AFR4N / HMA42GR7AFR4N Datasheet at 5, 7.

During the first mode (e.g., a normal mode of operation), the RCD uses the ALERT_n signal to indicate a parity error having occurred.

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

	After the DDR4RCD01 receives DPAR from the memory controller, it compares it with the data received on the CA inputs and indicates on its open-drain ALERT_n pin (active LOW) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[n:0]_n signals being LOW. The convention of parity is even parity, i.e., valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even. The DIMM-dependent control signals (DCKE0, DCKE1, DCS0_n .. DCS3_n, DODT0 and DODT1) are not included in the parity check computations. Even after a CA parity error has been registered, the device will still forward DCKEn and DODTn to the DRAMs, and the device will enter CKE power down mode depending on the DCKEn transitions. If a parity error occurs and parity checking is enabled in RC0E, the DDR4 register sets the 'CA Parity Error Status' bit in RCFx to '1'and disables parity checking. ALERT_n is asserted three input clocks after the erroneous command is registered. If the 'CA Parity Error Status' bit is '0', the DDR4 register logs the error by storing the erroneous command and address bits in the Error Log Register. ALERT_n stays asserted LOW until a 'Clear CA Parity Error Status' command is sent if the 'ALERT_n Assertion' bit in the Parity Control Word (RC0E) is '0'. In this case the erroneous command and all subsequent commands *See, e.g.*, JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;"

2.18 Control Words

The device features a set of control words, which allow the optimization of the device properties for different raw card designs. DDR4RCD01 control word (RCW) writes appear like DRAM MRS commands to MR7 which are ignored by the DDR4 DRAM. Each RCW write generates an MRS command to the rank 0 DRAMs behind the register, unless there is a parity error when parity checking is enabled, in which case both the RCW write as well as the MRS command to the DRAM are blocked. The different control words and settings are described below. Any change to these control words require some time for the device to settle. For changes to the control word setting, except for RC02 (DA3) and RC0A/RC3x, the controller needs to wait t_{MRD} after the last control word access, before further access to the DRAM can take place. For any changes to the clock timing (RC02: bit DA3, and RC0A/RC3x) this settling may take up to tSTAB time. All chip select inputs, DCS[n:0]_n, must be kept HIGH during that time.

The DDR4RCD01 allocates decoding for up to 16 4-bit words of control bits (RC00 through RC0F) and up to 15 8-bit words of control bits. Selection of each word of 4-bit control bits is presented on inputs DA4 through DA12. Data to be written into the 4-bit configuration registers need to be presented on DA0 .. DA3. Selection of each word of 8-bit control bits is presented on inputs DA8 through DA12. Data to be written into the 8-bit configuration registers need to be presented on DA0 .. DA7. Bits DA[16:14] must be LOW and at least one DCKEn input must be HIGH for a valid access. If register CKE power down feature is disabled, DCKEn inputs are don't care (either HIGH or LOW), and are forwarded to the QxCKEn outputs. The DODT[1:0] inputs are also don't care (can be either HIGH or LOW), and are forwarded to the QxODT[1:0] outputs. Address and command parity is checked during control word write operations unless parity is disabled in the Parity Control Word. ALERT_n is asserted and the command is ignored if a parity error is detected.

See JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode."

wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode.	The module controller of the SK hynix Products is, in the second mode, further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode. For example, the SK hynix products are configured to drive the Alert_n signal to the error edge connection via the open drain output while the memory module is in Clock-to-CA training mode, e.g., the second mode.

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode."

2.12 CA Bus Training Modes

The DDR4RCD01 supports several training modes (selected in Table 35, "RC0C: Training Control Word") in order to assist the memory controller in aligning the incoming command/address and control signals optimally to the input clock signal CK_t/CK_t. These training modes are only available if a non-zero latency adder has been selected.

In Clock-to-CA training mode the DDR4RCD01 ORs all enabled Dn inputs[1] every other cycle together and loops back the result to the ALERT_n output pin. In this mode, the DPAR input is sampled at the same time as the other Dn inputs. The ALERT_n latency relative to the DQn inputs is the same 3 cycles as in the normal parity mode. During any of the CA bus training modes, QCA/QxCKEn and QxODTn hold their previous values and parity checking is disabled.

The memory controller can use the Clock-to-CA training mode and feedback from the DDR4RCD01 to adjust the CK_t-CK_c to Dn relationship analogous to the write leveling sequence which adjusts the DQS-DQS_n to CK_t-CK_c relationship. The memory controller writes consecutive sequences of all '1's and all '0's on the CA bus and pulls in the Dn timing until the DDR4RCD01 samples all Dn inputs as 0, which is indicated with the LOW assertion of ALERT_n. This position indicates the start position of a cumulative CA bus "eye opening". The memory controller advances the clock position or pulls in the Dn timing until the DDR4RCD01 samples at least one input as '1', which is indicated by ALERT_n remaining high three cycles after the last command. This position indicates the end position of a cumulative CA bus "eye opening". The memory controller can now position either the clock phase or the Dn input timing so that the clock edge is in the middle of this "eye opening" to achieve equal amounts of setup and hold time relative to the clock edge.

Figure 22 shows three sampling phase positions where the loopback ALERT_n pin transmits either a consistent 0 output, a randomly toggling 1/0 output or a consistent 1 output, indicating sampling positions at the LOW time, the transition time or the HIGH time of the inputs, respectively.

The memory controller can use the DCS0_n, DCS1_n, DCKE0, DCKE1, DODT0 and DODT0 loop back modes in similar fashion. In each of these modes a single input signal is looped back to the ALERT_n output and the memory controller can determine the optimal clock position for each of the control signals that are used for a particular DIMM. Once the optimal clock position for all CMD/ADDR and control inputs has been established, the memory controller can determine the best clock position for the whole set of input signals or potentially move the timing of individual control signals around to increase either setup or hold margins relative to the clock edge.

See JEDEC RCD01 Specification (annotations added).

"wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode."

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

- CA Signals = QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2, QxPAR
- Control Signals = QxCKE0/1, QxODT0/1, QxC2, QxCS[1:0]_n for Dual CS mode, QxCS[3:0]
- CK = Yn_t - Yn_c

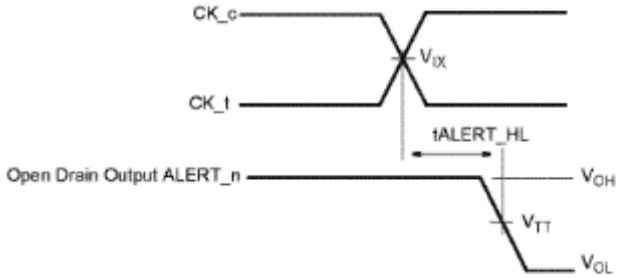


Figure 72 — Voltage waveforms, tALERT_HL Measurement

See JEDEC RCD01 Specification.

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode."

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	$V_{DD}/2$	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS[2] differential	Redriven clock
Reset output	QRST_n	CMOS[2]	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR QBPAR	CMOS[2]	Redriven parity[3]
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
	SDA	Open drain I/O	

See JEDEC RCD01 Specification (annotation added).

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode."

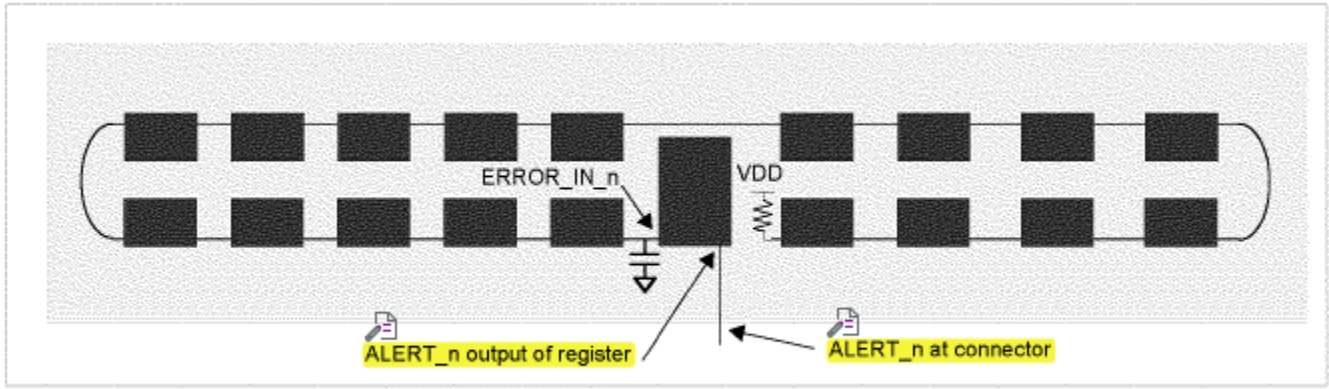


Figure 16 — Example Wiring of the ALERT_n Function

JEDEC RDIMM Standard (annotations added).

The Alert_n signals relate to the one or more training sequences. For example, while in Clock-to-CA training mode, the IDT 4RCD0124KC0 RCD ORs all enabled Dn inputs from the memory controller and then outputs the result of that OR operation to the memory controller via the Alert_n pin. The module controller of the SK hynix Products drives the open drain output and the error edge connection to one of two states.

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode."

2.12 CA Bus Training Modes

The DDR4RCD01 supports several training modes (selected in Table 35, "RC0C: Training Control Word") in order to assist the memory controller in aligning the incoming command/address and control signals optimally to the input clock signal CK_t/CK_t. These training modes are only available if a non-zero latency adder has been selected.

In Clock-to-CA training mode the DDR4RCD01 ORs all enabled Dn inputs[1] every other cycle together and loops back the result to the ALERT_n output pin. In this mode, the DPAR input is sampled at the same time as the other Dn inputs. The ALERT_n latency relative to the DQn inputs is the same 3 cycles as in the normal parity mode. During any of the CA bus training modes, QCA/QxCKEn and QxODTn hold their previous values and parity checking is disabled.

The memory controller can use the Clock-to-CA training mode and feedback from the DDR4RCD01 to adjust the CK_t-CK_c to Dn relationship analogous to the write leveling sequence which adjusts the DQS-DQS_n to CK_t-CK_c relationship. The memory controller writes consecutive sequences of all '1's and all '0's on the CA bus and pulls in the Dn timing until the DDR4RCD01 samples all Dn inputs as 0, which is indicated with the LOW assertion of ALERT_n. This position indicates the start position of a cumulative CA bus "eye opening". The memory controller advances the clock position or pulls in the Dn timing until the DDR4RCD01 samples at least one input as '1', which is indicated by ALERT_n remaining high three cycles after the last command. This position indicates the end position of a cumulative CA bus "eye opening". The memory controller can now position either the clock phase or the Dn input timing so that the clock edge is in the middle of this "eye opening" to achieve equal amounts of setup and hold time relative to the clock edge.

Figure 22 shows three sampling phase positions where the loopback ALERT_n pin transmits either a consistent 0 output, a randomly toggling 1/0 output or a consistent 1 output, indicating sampling positions at the LOW time, the transition time or the HIGH time of the inputs, respectively.

The memory controller can use the DCS0_n, DCS1_n, DCKE0, DCKE1, DODT0 and DODT0 loop back modes in similar fashion. In each of these modes a single input signal is looped back to the ALERT_n output and the memory controller can determine the optimal clock position for each of the control signals that are used for a particular DIMM. Once the optimal clock position for all CMD/ADDR and control inputs has been established, the memory controller can determine the best clock position for the whole set of input signals or potentially move the timing of individual control signals around to increase either setup or hold margins relative to the clock edge.

See JEDEC RCD01 Specification (annotations added).

U.S. Patent No. 10,474,595: Claim 10

"wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode."

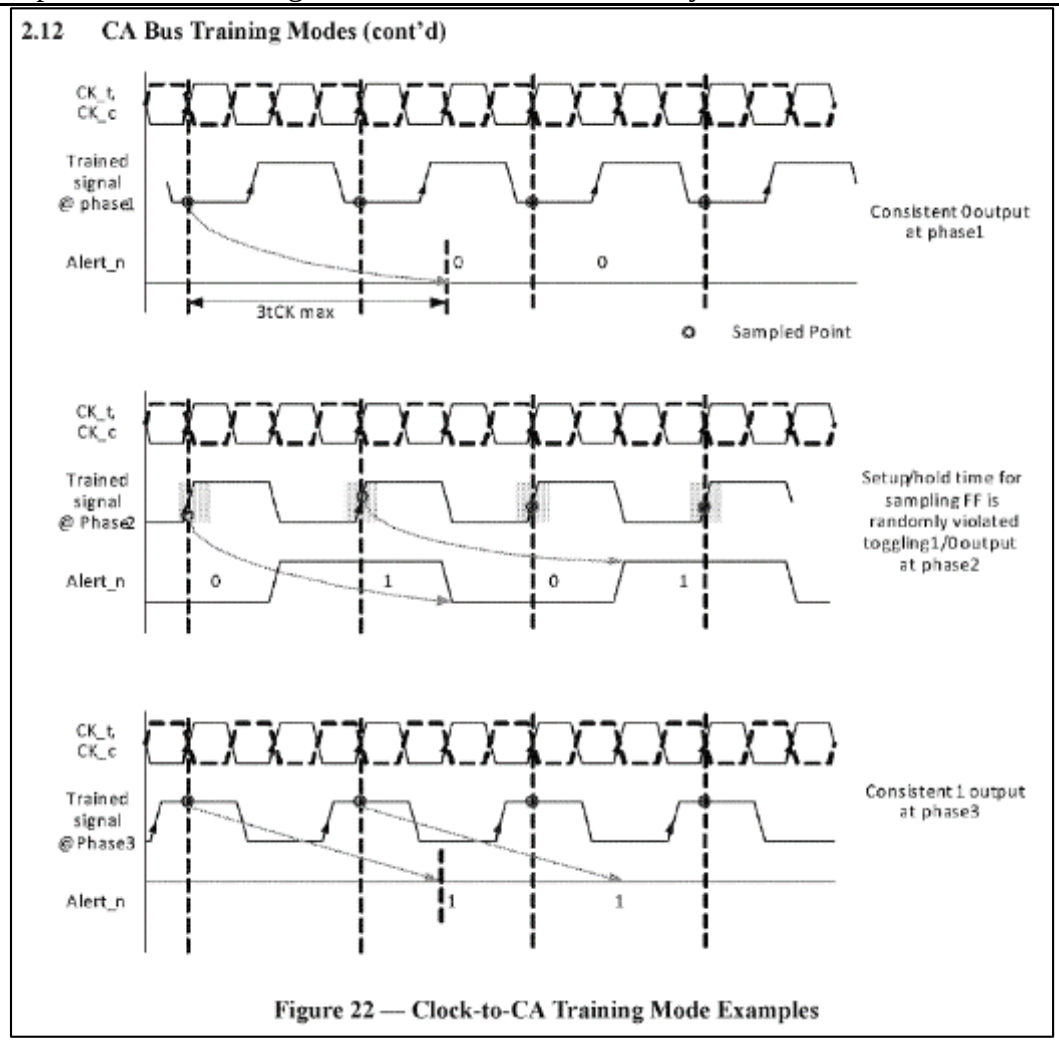


Figure 22 — Clock-to-CA Training Mode Examples

See JEDEC RCD01 Specification.